IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	)	C.A. No. 06-788 (JJF)

FREESCALE'S OPENING CLAIM CONSTRUCTION BRIEF

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INTRODUCTION

Freescale Semiconductor, Inc. ("Freescale") is a global leader in the design and manufacture of semiconductor products for the automotive, consumer, industrial, networking and wireless markets. After more than 50 years as Motorola's in-house semiconductor products sector, Freescale was spun off in July 2004. Based in Austin, Texas, Freescale has operations for design, research and development, manufacturing and sales in more than 30 countries. Its semiconductor components are used in well-known consumer products, such as Motorola cell phones, Sony electronics, Whirlpool appliances, Life Fitness cardiovascular and strength training equipment, Cisco routers, Bose Acoustic Wave radios, and many motor vehicles.

Freescale and its engineers have received important recognition for innovation. For example, the U.S. Commerce Department awarded Motorola (then including Freescale) the 2004 National Medal of Technology for "75 years of technological achievement and leadership in the development of innovative electronic solutions, which have enabled portable and mobile communications to become the standard across society." The U.S. Patent Office has granted Motorola and Freescale over 5,000 patents relating to semiconductor technology.

In the early 1990's, Motorola (later Freescale) was a leading manufacturer of DRAM (i.e., the key kind of memory for computers). Motorola applied for and received numerous DRAM patents on its groundbreaking innovations. The early 1990's marked an increase in competition from foreign DRAM manufacturers who, instead of developing their own technologies, copied technology of industry leaders such as Freescale, and then undercut U.S. DRAM manufacturers' prices. In response, Freescale stopped making memory products and instead focused on semiconductor products. Nevertheless, because Freescale had developed a valuable DRAM patent portfolio, nearly all of the top worldwide DRAM manufacturers took a license to use Freescale's patented DRAM technology.

ProMOS, however, refused to license the Freescale technology it was using. After years of fruitless negotiations where ProMOS kept stalling, Freescale filed a patent infringement lawsuit against ProMOS in the Eastern District of Texas. ProMOS filed this suit in retaliation.

ProMOS is asserting three patents against Freescale: the Fortin patent directed to part of a process for manufacturing semiconductor chips, and two Chan patents directed to cache memory products. ProMOS admittedly does not use these patents. Neither does Freescale. To try to reach Freescale's different technology, however, ProMOS is attempting to stretch the meaning of the claims well beyond the meanings used and disclosed by Fortin and Chan.

THE FORTIN PATENT

I. STATEMENT OF FACTS

A. Chip Fabrication Technology

Semiconductor "chips" are used in electronics to quickly and compactly perform numerous electrical operations. Using well-known fabrication processes, chips are made by Freescale and other chip manufacturers by placing a large number of tiny components, such as transistors and capacitors, on a single semiconductor wafer. Thin layers of metal are deposited to form the connections among those components to create individual electrical circuits within the chip. These metal layers are separated by electrically insulating layers.

For a chip to function as desired, electrically conductive paths (sometimes called "plugs") must connect the metal layers through the intervening insulating layers to form a complete, functional "integrated circuit." One way that plugs are made is to first create holes (also called "contact openings" or sometimes "vias") in the insulating layer and then to fill the holes with a conductive material before depositing the next metal layer. Tungsten is a metal (thus a conductive material) widely used to fill contact openings.

The four basic, well-known steps involved in making a tungsten plug for an integrated

circuit include: (i) forming an insulating layer over a metal layer, (ii) creating a contact opening in the insulating layer to expose the metal layer underneath the insulating layer, (iii) forming a "barrier" layer (typically made of titanium nitride ("TiN") or a combination of titanium ("Ti") followed by TiN) over the insulating layer that extends into the contact opening, and (iv) filling the contact opening with tungsten. The tungsten plug forms a conductive path connecting the metal layer underneath the insulating layer to the metal layer then added on top of the insulating layer.[1] The TiN barrier layer (formed in step (iii) above) is a "barrier" in the sense that, although electrically conductive, it protects the surrounding insulating layer (or Ti layer where the barrier layer consists of both Ti and TiN) from chemically reacting with the subsequently deposited tungsten. (Chang, et al., *Effects of Barrier–Metal Schemes of Tungsten Plugs and Blanket Film Deposition*, at 4738 (Ex. B); Herner, et al., *"Volcano" Reactions in Oxide Vias Between Tungsten CVD and Bias Sputtered TiN/Ti Films*, at 1982 (Ex. C)). Freescale, its predecessor Motorola, and other chip manufacturers have been following these basic steps to fabricate chips for decades. The Fortin patent claims certain alleged improvements in one way of carrying out these common steps – a way that the accused processes do not use.

Of particular focus in this litigation is the formation of the barrier layers of TiN. The two main techniques for doing so are physical vapor deposition ("PVD") and chemical vapor

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[1] The background section of Fortin describes these well-known steps: step 1 deposits a "dielectric" layer (i.e., nonconductive or insulating layer) over a metal or silicon layer; in step 2, "A via is etched in the dielectric" (i.e., a hole is made in the insulating layer); step 3 deposits a titanium layer and then a TiN layer; in step 4, a tungsten layer is deposited to complete the formation of the plug, after which another metal layer is deposited (Ex. A at 1:25–39).

The exhibits cited in this brief are in appendices of exhibits filed herewith in separate volumes for Fortin (lettered exhibits) and Chan (numbered exhibits). At TAB 1 attached to this brief are claim charts of the terms in dispute; TAB 2 provides a grouping of the similar Chan terms in dispute.

deposition ("CVD"). (Plummer, et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000), at 511 (Ex. D)). PVD and CVD are well known and have been used for decades to deposit materials in a variety of applications, including layers during chip fabrication. (Wang, et al., *Enhanced Metalorganic Chemical Vapor Deposition Titanium Nitride Film Fabricated Using Tetrakis-Demethylamino-Titanium for Barrier Metal Application in Sub-Half-Micron Technology*, at 4274 (Ex. E)). "In each case, the silicon wafer is placed in a deposition chamber, and the constituents of the [layer to be deposited] are delivered through the gas phase to the surface of the substrate where they form the [layer]" (Ex. D, Plummer at 511). In other words, both processes, using a vapor, deposit material to build up a layer. The mechanisms of action, however, differ in the two processes. As their names suggest, PVD involves physical mechanisms while CVD involves chemical reactions: "In the case of *CVD*, reactant gases are introduced into the deposition chamber, and *chemical reactions between the reactant gases [taking place] on the substrate surface* are used to produce the [layer]. In the case of *PVD*, *physical methods are used to produce the constituent atoms* which pass through a low-pressure gas phase [vapor] and then *condense*[2] on the substrate." (*Id.*; *see also* Wolf, et al., *Silicon Processing for the ULSI Era (2000)*, at 149 (CVD), 434 (PVD) (Ex. F)).

A common example of PVD is "sputtering," which involves a particular way of converting into a vapor the material to be deposited, i.e. through bombarding a "target" surface of the material, thereby dislodging atoms from the surface of the target to form the vapor which then condenses on the substrate (Ex. F, Wolf at 434). For example, sputtering is often used to form a vapor of TiN from a solid target (*Id.* at 438).

In the fabrication of barrier layers using CVD, a common starting chemical material is

[2] Condensation is a physical mechanism also.

$TiCl_4/NH_3$ (used by prior art cited in the prosecution history) or TDMAT (a material containing titanium, which the accused processes use). One product of the chemical reaction of these starting materials during CVD is TiN, which accumulates on the insulating layer surface.

CVD techniques are often followed by a N_2/H_2 treatment (called a "plasma" treatment) to remove contaminants in the barrier layer leftover from the $TiCl_4/NH_3$ or TDMAT starting material. This plasma treatment improves the conductivity and reduces the thickness of the deposited barrier layer by removing the contaminants.

In addition to the steps outlined above, it is common to include a "pre-clean" step, usually involving a plasma etch, to clean the contact opening prior to forming the barrier layer (i.e., between steps ii and iii, above). After forming the barrier layer, it is also common to "anneal" (or heat) the barrier layer (between steps iii and iv, above) in a nitrogen atmosphere to improve barrier layer durability as well as adhesion of the tungsten plug to the barrier layer.

PVD techniques for forming TiN barrier layers have been popular since the early 1990's because of their relatively low cost and ease of production. As chips have become smaller and smaller, however, manufacturers have faced problems with TiN barrier layers formed by PVD. (Ex. E, Wang at 4274; Ex. B, Chang at 4738). These problems stem from the inconsistent, non-uniform deposition of the TiN barrier layer at different points within the contact openings, also known as poor "step coverage," which lead to weak or failing barrier layers.[3] (Ex. E, Wang at 4274; Ex. B, Chang at 4738; Ex. C, Herner at 1982).

Chip manufacturers have generally addressed poor step coverage in contact openings in

[3] Step coverage refers to the quality and uniformity of barrier layer formation within the contact opening. It generally decreases as contact holes get deeper while the openings at the top of the hole get narrower, such that poor, or inadequately weak, barrier layers form on the sidewalls or bottom corners of a contact hole.

one of two ways: (1) improving step coverage and barrier layer durability for existing PVD techniques (*see* Ex. C, Herner at 1982), as Fortin sought[4]; or (2) using CVD instead of PVD**,** as in Freescale's accused HiP7 and HiP8 processes. CVD provides much better step coverage in the contact opening than PVD. (Ex. E, Wang at 4274; Ex. B, Chang at 4738).

B. Fortin's Specific PVD Process

Vincent Fortin filed his patent application in this well-developed field on June 13, 2001. Fortin discloses and claims a process for fabricating tungsten plugs using TiN barrier layers of a certain thinness formed by PVD ('267 patent *see, e.g.*, the abstract and claim 1 (Ex. A)). There can be no question that Fortin's invention is limited to the formation of TiN layers by PVD. Indeed, the Fortin patent is titled "Formation of Tungsten-Based Interconnect Using *Physically Vapor Deposited* Titanium Nitride Layer" and the patent's specification begins: "The present invention relates to *physical vapor deposition* of titanium nitride" (Ex. A at 1:8–9) (emphasis added). Describing the prior art, Fortin acknowledged that it was known to form TiN barrier layers by CVD: "Titanium nitride layer 150 can be deposited by a number of techniques, including sputtering and chemical vapor deposition (CVD)" (Ex. A at 1:40-42). But he claimed as his invention forming TiN barrier layers *only* by PVD techniques. Every claim of the patent specifically limits the TiN deposition step to PVD, with certain claims directed to the particular PVD process of sputtering[5] (Ex. A).[6]

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[4] Fortin referred to the problem as the presence of "volcanoes" or "voids."

[5] This should not be confused with the formation of the tungsten layer by CVD, which the patent also claims. It is the use of PVD for the TiN layer that presents the key issue for claim construction, although Freescale and ProMOS agree that CVD also requires construction.

[6] A representative claim of Fortin is claim 1: "A fabrication method comprising: providing a structure with an opening that extends partway through the structure, the opening having a parametrical top edge that extends along an exterior surface of the structure; rounding the top edge of the opening; forming a titanium nitride layer over the structure by physical vapor (Continued . . .)

That Fortin is limited to forming the TiN layer by PVD was explicitly reaffirmed during prosecution. The Examiner initially rejected most of Fortin's claims over U.S. Pat. No. 5,420,072 to Fiordalice ("Fiordalice"), which discloses fabrication of TiN barrier layers as thin as those claimed by Fortin (using $TiCl_4/NH_3$ as the starting material). (Ex. G, at 3-7). In response, Fortin argued successfully that his invention was patentable because Fiordalice discloses forming a TiN layer by *CVD*, whereas his invention forms the TiN layer by *PVD:* "Fiordalice discloses that layers 22 and 24 are formed by chemical vapor deposition ("CVD"), not physical vapor deposition ("PVD") (Ex. H at 9; *see also id.* at 9-10) ("Since Fiordalice discloses that titanium nitride layers 22 and 24 are formed by CVD, . . . Fiordalice cited by the Examiner in regard to deposition of the titanium nitride layer, does not disclose the limitation of [Fortin] Claim 1 that the titanium nitride layer be formed by PVD to a thickness of less than 30 nm.") (original emphasis). To drive home the point, Fortin emphasized, "In any event, CVD is not PVD or a type of PVD." (Ex. H at 9) (emphasis in original).

As part of his argument, Fortin confirmed his ordinary use of the terms (Ex. H at 9) (emphasis in original). He characterized PVD as:

> [a] general term for a deposition process in which the material to be deposited is released from the source of the material largely by one or more physical mechanisms.

He characterized CVD as:

> [a] deposition process in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be

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(. . . continued)
deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 25 nm thick; heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening."

> deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface.

Later, the Examiner rejected all claims over a second reference, U.S. Pat. No. 6,110,789 ("Rhodes"), which disclosed all of the claimed process steps, including forming TiN layers by PVD to the required thinness (Ex. I at 3-5). Fortin then amended his claims to include a "rounding" limitation in each of the independent claims prior to forming the TiN layer and argued for patentability over Rhodes based on "rounding" (Ex. J at 8-11):

> In short, the top-edge rounding act recited in Claim 1 or 38 is not merely an act performed as a matter of design choice. Instead, the rounding act is a significant factor in achieving the volcano-reduction objective of the invention . . . The absence of such a disclosure or suggestion combined with the significant nature of the rounding act in Claim 1 or 38 is further reason why Claims 1 and 38 are patentable.

In his disclosure, however, Fortin does not teach how such "rounding" achieves the stated objective of improving barrier layer durability, how "rounding" should be measured, or what degree of "rounding" is necessary to achieve that objective. Indeed, he states that, "Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers . . ." (Ex. A at 1:67-2:5). Further, Fortin also describes the anneal step as contributing to the objective of improved durability of the barrier layer (Ex. A at 4:13-17), such that it is not clear how effective or essential "rounding" is to achieving that objective when used in combination with effective anneal parameters, or how much rounding is necessary under these circumstances. That is, nothing in the disclosure teaches or suggests what combination of the rounding and anneal steps would achieve the stated objective of improving the durability of the barrier layer; nor does the disclosure include how such a determination should be made.

II. FORTIN CLAIM CONSTRUCTIONS

Claim construction is a question of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977-78 (Fed. Cir. 1995), *aff'd* 517 U.S. 370, 388-90 (1996).

A claim term should be construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Id.* at 986. Unless the inventor clearly supplies a different meaning, courts should interpret the language of the claim by applying the ordinary and customary meaning of the words in the claims. *Prism Techs. LLC v. Verisign, Inc.*, 2007 WL 988564, at *1 (D. Del. Apr. 2, 2007) (citing *Envirotech Corp. v. Al George, Inc.*, 730 F. 2d 753, 759 (Fed. Cir. 1984)).

Claim construction must be based on the context of the entire patent, including the specification and claims. *Phillips v. AWH Corp*, 415 F.3d 1303, 1313-17 (Fed. Cir. 2005). The prosecution history may also provide guidance as to the meaning of the claim terms and inform how the inventor understood the invention, including whether the inventor limited the invention in the course of prosecution to make the claim scope more narrow. *Id.* at 1317; *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005). A court may consider the extrinsic evidence, including expert and inventor testimony, dictionaries, and learned treatises, for assistance in understanding the technology, the meaning of terms to one skilled in the art, and how the invention works. *Phillips*, 415 F.3d at 318-19.

A. "physical vapor deposition" and "chemical vapor deposition"[7]

The terms PVD and CVD have well-established meanings as noted above, and Fortin's usage in the claims and specification is entirely consistent with their ordinary meaning. Moreover, Fortin made clear during prosecution that he was using those well established

[7] The claim chart at TAB 1 identifies the claims in which the disputed Fortin terms appear.

meanings and that the processes are mutually exclusive, i.e., a process can be one or the other, not both.

The ordinary meanings of PVD and CVD include at least three essential notions relating to their end result and way of achieving the end result. First, as the terms on their face require and as is clear from the purpose of PVD and CVD, both result in the "deposition" of material on a surface, i.e., that material accumulate (Fortin's term) or build up on a surface. The accumulation or building up of material is a fundamental feature of deposition processes, as is clear from all the cited references above and the patent itself, and it distinguishes them from, for example, removal processes such as cleaning or etching, which remove material.

Second, as noted above, CVD and PVD involve the deposition of material out of a "vapor" or gas phase to form a solid film on the deposition surface.

Third, the processes involve certain mechanisms of action. In the case of PVD, the material is *released by physical action* from a source and then deposited on the surface. In the case of CVD, *chemical reactions between the starting reactant gases on the substrate surface* produce the material deposited on the surface. (Ex. E, Wolf at 149 (CVD), 434 (PVD)).

As explained below, Freescale's proposed definitions of PVD and CVD address and make clear these essential aspects and the distinguishing features of the processes, while ProMOS's do not. Moreover, Freescale's proposed definitions include the essential and incontestable notion that CVD and PVD are distinct (as Fortin represented to the Patent Office in order to obtain issuance of the patent), while ProMOS's proposed constructions do not.

"physical vapor deposition"	
Freescale's construction of PVD	ProMOS's construction of PVD
A process of building up material on a surface in which the material to be deposited is released from a source of the material into a vapor phase by one or more physical mechanisms. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	A process in which films are deposited atomically by means of fluxes of individual neutral or ionic species.

"chemical vapor deposition"	
Freescale's construction of CVD	ProMOS's construction of CVD
A process of building up material on a surface in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	A process in which films are precipitated from the gas phase by a chemical reaction

First, Freescale's definitions include explicitly that CVD and PVD are processes of "building up material on a surface." ProMOS's definition of PVD recites the word "deposition," but does not define it. ProMOS's definition of CVD is even less helpful because not only does it fail to provide a meaning for deposition, it does not even include the term "deposition," as does its PVD definition. "Deposition" is a term that a jury should not have to wonder about when its definition is easily understood. Its ordinary meaning conveys the notion of building up or accumulating on a surface, a notion ProMOS's definition would ignore. Fortin himself in the prosecution history spoke of "accumulation" of the material on the surface (Ex. H at 9).

Freescale's definition of "deposition" within its constructions for PVD and CVD is also consistent with other words in the claims (*see*, *e.g.*, Claim 1: "*forming* a titanium nitride layer . . .by physical vapor deposition"). That is, the claimed deposition processes result in the *formation* of a layer such that the layer builds up to a desired thickness during its formation. *Phillips*, 415 F.3d at 1314 ("[T]he context in which a term is used in the asserted claim can be highly instructive"); *see also ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms"). Nothing in the claims suggests that deposition should include a step in which a layer is not formed, but is etched (e.g. with a plasma treatment), for example, a notion which ProMOS transparently seeks to include.

Second, both processes, as their names suggest, involve deposition of material from a

"vapor" (i.e., the gas phase of a compound). In PVD, the material to be deposited is released from a starting material into a vapor by a physical mechanism (such as sputtering or evaporation), and then deposited (often by a physical mechanism, such as condensation). In CVD, there is a starting chemical species in a vapor form, and the material to be deposited is released from that species by chemical reaction on the deposition surface (pp. 3-4, *supra*). Freescale's definitions make clear that there is a vapor in both CVD and PVD, and its proper place in the process. ProMOS's definition of PVD instead uses an obtuse term, "flux," partially addressed to the characteristics of the material during the process (the material flows), but which the jury will not understand and which does not even necessarily have to be a vapor. (All "flux" means is that the material flows, which is true for liquids and gases. *See, e.g. Webster's New College Dictionary*.) That ProMOS's definition of CVD does at least reference "gas phase" only emphasizes that its definition of PVD is flawed in failing to include the requirement of a "vapor."

Third, Freescale's definitions distinguish between the mechanisms of action for releasing material from a starting material in PVD and CVD. In fact, Freescale's definitions closely parallel Fortin's descriptions of the mechanisms of action filed during prosecution, as noted above (pp. 7-8, *supra*). ProMOS's definition, particularly of PVD, obfuscates the mechanism of action by use of new, obscure terminology nowhere used by Fortin, "deposited atomically by means of fluxes of individual neutral or ionic species." ProMOS's definition of CVD as requiring a chemical reaction is more understandable, and closer in meaning to the usual terminology (and Freescale's proposed construction mirroring Fortin's language), but it is not a complete definition for other reasons as noted above. ProMOS's definition does not improve upon the description Fortin himself gave of the requirement of a chemical reaction.

Finally, Fortin's successful efforts to overcome the prior art cited by the Examiner make clear that Freescale's inclusion of what PVD is not (i.e. CVD) is entirely proper. That is, the prosecution history makes clear that the release of material in PVD is by physical, not chemical, action and that CVD is not PVD (Ex. H at 9):

"CVD is a deposition process in which . . .the material to be deposited undergoes suitable <u>chemical reaction</u> to be released from the starting chemical species and accumulate on the deposition surface."	**"PVD is a general term for a deposition process in which the material to be deposited is released from the source of the material largely by one or more <u>physical</u> mechanisms"**
"In any event, CVD is <u>not</u> PVD or a type of PVD."	

(original emphasis). Accordingly, the definitions here properly should include the distinction urged by the inventor that "CVD is not PVD." *See Applied Science & Tech., Inc. v. Advanced Energy Indus., Inc.*, 204 F. Supp. 2d 712, 715 (D. Del. 2002) (construing disputed limitation in a manner defining what the invention does <u>not</u> encompass based on specification and prosecution history) (*citing SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1345 (Fed. Cir. 2001)); s*ee also Phillips*, 415 F.3d at 1317 ("Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent.").

Only Freescale's definitions reflect the well established meanings of PVD and CVD in the art, and are consistent with their use by Fortin in the patent and his characterizations during prosecution. ProMOS's definitions, on the other hand, would vitiate the claims by improperly omitting various requirements of PVD and CVD. *See Oak Tech., Inc. v. Int'l Trade Comm'n*, 248 F.3d 1316, 1328-29 (Fed. Cir. 2001) (courts cannot read out a limitation imposed by the claim) (*citing Texas Instruments Inc. v. United States Int'l Trade Comm'n*, 988 F.2d 1165, 1171 (Fed. Cir. 1993) ("To construe the claims in the manner suggested [by the patentee] would read an express limitation out of the claims. This we will not do because 'courts can neither broaden nor narrow claims to give the patentee something different than what he has set forth.").

B. "sputtering"

Freescale's Proposed Construction	ProMOS's Proposed Construction
A type of physical vapor deposition in which a solid target is bombarded with high energy ions physically to dislodge the surface atoms on the target into a vapor phase for accumulation on the deposition surface without undergoing a chemical reaction.	A process in which atoms from near the surface of a material are physically dislodged by an incoming ion.

Unquestionably, "sputtering" is well understood in the art as a particular type of PVD. The Wolf reference, for example, says that "sputtering . . . is the primary PVD method utilized in [certain chip fabrication] applications" (Ex. F at 434). The particular aspect of sputtering as a PVD method is how it generates the vapor without a chemical reaction. Freescale's definition makes clear that sputtering is a type of PVD and then includes the way that sputtering forms the vapor of the material to be deposited (by bombarding the target). ProMOS's definition, however, while addressing the beginning part of the process with the dislodgement of atoms from a surface, says nothing about the rest of the process. It omits that sputtering is a PVD process, including that the atoms are dislodged into a vapor phase and that it is a deposition process accumulating material on the deposition surface.

There can be no question that Fortin uses "sputtering" in its traditional way as a PVD process. In dependent claims 2, 32, 48, and 54, sputtering is claimed by reference to independent claims 1, 31, 47, and 52 as the particular physical vapor deposition process by which TiN layers are formed. *See, e.g.*, Ex. A at 5:12-13 ("the method of claim 1 wherein the titanium nitride layer is formed by sputtering"). In independent claim 25, sputtering is claimed for forming the TiN layer. *Phillips*, 415 F.3d at 1314 ("Because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims.") (internal citations omitted).

The specification consistently describes the invention as directed to PVD of TiN (*see* pp. 6-8, *supra*) and makes clear that sputtering is a type of PVD: "The invention is not limited to

any particular sputtering process, and further is applicable to TiN deposited by physical vapor deposition techniques other than sputtering" (Ex. A at 4:49-52). If there were any doubt, Fortin removed it when, during prosecution, he stated that "sputter deposition is a type of PVD" (Ex. H at 10; *see also id.* at 11).

Freescale's definition of sputtering within the framework of physical vapor deposition is thus compelled by the patentee's own use of the term consistent with its use in the art. ProMOS's definition is incomplete and has no foundation in the art or the intrinsic record.

C. "rounding"

Freescale's Proposed Construction	ProMOS's Proposed Construction
This term is indefinite.	Reducing the sharpness of the top edge of the opening.

Independent claims 1, 25, 31, and 47 include the limitation "rounding the top edge of the opening" while dependent claims 18 and 42 include variations thereof. Because the claims with the "rounding" limitation do not reasonably apprise one of ordinary skill in the art of their scope, the claims are indefinite.

Section 112, ¶ 2 requires patentees to "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." Under § 112, ¶ 2, a claim must allow one skilled in the art to determine "the bounds of the claim when read in light of the specification." *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002). That is, the focus of a § 112, ¶ 2 inquiry is "whether the claims, as interpreted in view of the written description, adequately perform their function of notifying the public of the [scope of the] patentee's right to exclude." *Honeywell Int'l, Inc. v. ITC*, 341 F.3d 1332, 1338 (Fed. Cir. 2003). Analysis of claim indefiniteness is a question of law that is properly considered at the time of claim construction. *See Atmel Corp. v. Info. Storage Devices*, 198 F.3d 1374, 1379 (Fed. Cir. 1999) (indefiniteness analysis is "inextricably intertwined with claim construction").

The "rounding" limitation renders the claims indefinite because it does not permit one skilled in the art to determine the bounds of the claims in light of the specification and, therefore, to assess or avoid infringement. The specification describes the desirability of rounding the top edges of the claimed opening prior to TiN deposition to allegedly reduce stress in the TiN barrier layer and improve the durability of the barrier layer (Ex. A at 2:59-3:2). It further discloses, however, that preferred annealing parameters contribute to improved durability in TiN barrier layers as well (Ex. A at 4:13-17).

Nothing in the patent teaches, suggests, or claims the degree of rounding required to achieve the stated objective, or how, or against what baseline, such a measurement would be made so that a competitor or other potential infringer could determine whether the limitation is satisfied. *Amgen Inc. v. Hoechst Marion Roussel*, 314 F.3d 1313, 1342 (Fed. Cir. 2003) (claims must be "sufficiently precise to permit a potential competitor to determine whether or not he is infringing.") (internal citations omitted). Nor does ProMOS's construction ("reducing the sharpness of the top edge of the opening") cure the uncertainty. Rather, by introducing a subjective quality (sharpness) to a competitor's determination of whether the limitation is met, ProMOS confirms its indefinite nature. Furthermore, trying to determine the amount of rounding necessary to achieve the stated objective would be particularly futile in light of Fortin's disclosure of the contribution of proper annealing parameters to achieving the stated objective. *Id.* (finding indefinite a claim requiring comparison to moving target since the patent failed to direct those of ordinary skill in the art to a standard by which the appropriate comparison could be made). For all of these reasons, the term "rounding" is fatally indefinite.

THE CHAN PATENTS

I. CHAN TECHNOLOGY

The Chan patents relate to cache technology. U.S. Pat. No. 5,488,709 ("the '709 patent") is directed to a cache chip and is titled "Cache Including Decoupling Register Circuits." U.S. Pat. No. 5,732,241 ("the '241 patent") is directed to a system that includes a cache chip and a cache controller and is titled "Random Access Cache Memory Controller and System."

Both the '709 and '241 patents claim priority to the same abandoned patent application, and only the Abstract and 15 lines in the Summary of the Invention differ between the two patents. The remaining differences are cosmetic.[8] Because the specifications are essentially the same, for convenience the '709 specification will be cited.

The claims for both patents were rejected by the Patent Office several times. Consequently, Chan had to significantly narrow his claims before convincing the Patent Office to issue his patents. As also described below, the Chan patents were expressly directed to two specific semiconductor chips; indeed a large portion of the specification for the Chan patents was copied verbatim from product literature for those two products.

A. Cache Memory

A cache is a memory device into which frequently used data is duplicated so that the data can be more quickly accessed by a computer's central processing unit (CPU) (Ex. 3, *i486 Microprocessor Hardware Manual,* at 6-1).[9] The cache stores some of the same data stored in the computer's main memory (also known as "system" memory). (*Id.*) The cache is located

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[8] The '709 specification is 78 columns while the '241 is only 64 columns because "Table I" and "Table II" were printed in single-column format in the '709 patent (*see* Ex. 6 at 10:56-32:36) but in dual-column format in the '241 patent (*see* Ex. 7 at 10:48-22:54).

[9] A CPU is also known as "processor," "microprocessor," or "host." In fact, those terms are used interchangeably in the Chan specification. *See infra* Part IV.F.

closer to the CPU and is a type of memory that has faster access than system memory. (*Id.*) Using a cache thus allows the computer to operate faster because frequently accessed information can be retrieved more quickly from the cache than from the slower main/system memory. (*Id.*)

When the CPU wishes to read or write data to or from a particular main memory address, a check is made to determine whether the cache has a copy of the requested memory location. (*Id.* at 6-2.) If so, then what is known as a "cache hit" occurs. (*Id.*) If the cache does not have a copy of that memory location, then what is known as a "cache miss" occurs. (*Id.*)

In the case of a "cache miss," the CPU has to access system memory to either read or write the data. (*Id.*) Accessing system memory slows down the CPU because system memory operates at a much lower frequency (*i.e.*, fewer cycles per second) than the CPU. (*Id.*) The CPU has to stop its operation to wait for the slower system memory to read out or write data. (*See id.)*

In the case of a "cache read hit," the CPU can read the data from the cache much quicker than it can with system memory. (*Id.*) For a "cache write hit," data that has been modified by the CPU is saved to the cache. (*Id.* at 6-11.) At some point, this modified data must also be saved (*i.e.*, written back) to system memory. (*Id.*)

The timing of the modified data being written back to system memory depends on whether the applicable cache is "write-back" or "write-through." (*Id.*) In a "write-through cache," every time the CPU writes to the cache, the data is also written to the underlying system memory location. (*Id.*) In a "write-back cache," the cache instead tracks which of its locations have been written over with modified data, and marks these locations "dirty" (*i.e.*, the data is modified but was not yet saved to system memory). (*Id.* at 6-12.) Because a cache has limited size, when new data is to be saved to the cache, other data must often be "evicted" or

"evacuated." (*See id.*) If the data to be evicted is marked "dirty," that gets written-back to system memory. (*Id.*)

The table below provides a glossary of the basic cache-related terminology:

cache	a memory element (usually SRAM) that stores data that is frequently used by the central processing unit
CPU	also called the central processing unit, processor, microprocessor, or host, it is the "brains" of the computer
system memory	also called main memory, it is the memory (usually DRAM) that stores the data needed by the CPU
cache write hit	CPU wants to write to a particular address in system memory and that address is found (*i.e.*, "hit") in the cache, so that the CPU can write data to the cache
cache read hit	CPU wants to obtain data from a particular address in system memory and that address is found in the cache, so the CPU is able to obtain that data quickly from the cache
cache write miss	CPU wants to write to a particular address in system memory, but that address is not found (*i.e.*, "miss") in the cache, so the CPU has to access system memory to store the data
cache read miss	CPU wants to obtain data from a particular address in system memory, but that address is not found (*i.e.*, "miss") in the cache, so the CPU has to access system memory to obtain the data
write-back cache	when a write is made to system memory at a location that is currently cached, the new data is written only to the cache, not actually written to the system memory. Later, if another memory location needs to use the cache line where this data is stored, it is saved ("written back") to the system memory and then the line can be used by the new address.
write-through cache	every time the processor writes to a cached memory location, both the cache and the underlying memory location are updated.
dirty or "dirty bit"	indicator (often a single bit of memory) that indicates whether the cache location contains data that has been modified and thus must be written-back to system memory
evacuation or eviction	removing data from the cache to make room for new data

B. Internal vs. External Cache

A cache may be internal or external to the CPU. (*See id.* at 1-2.) A cache that is "internal" is part of the same integrated circuit (or "IC") as the CPU, which means they both are on the same semiconductor chip. (*See id.*) An internal cache (in grey) is shown in Figure 2-1 below, which is a page from the reference manual for a particular CPU, the Intel 80486. (*Id.* at 2-2.) Figure 2-1 illustrates the internal components of the CPU (within gold area), which is the same "i486 Processor" depicted in Figure 1-4. (*Id.* at 1-9.) The Chan patents properly acknowledge that the 80486 microprocessor includes an internal cache, and that this internal cache is prior art to the Chan patents. ('709 at 2:66-3:1; 3:17-32).

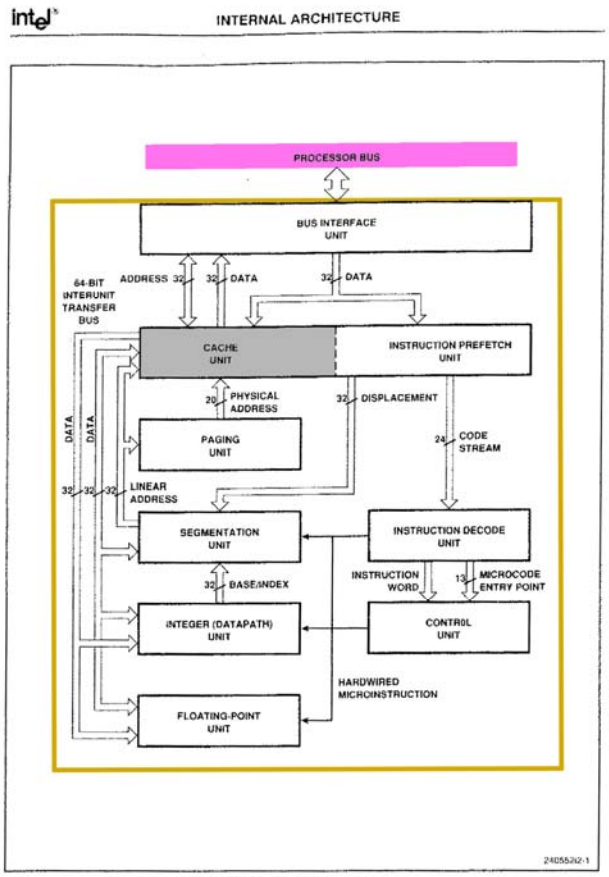


Figure 2-1. Internal Architecture

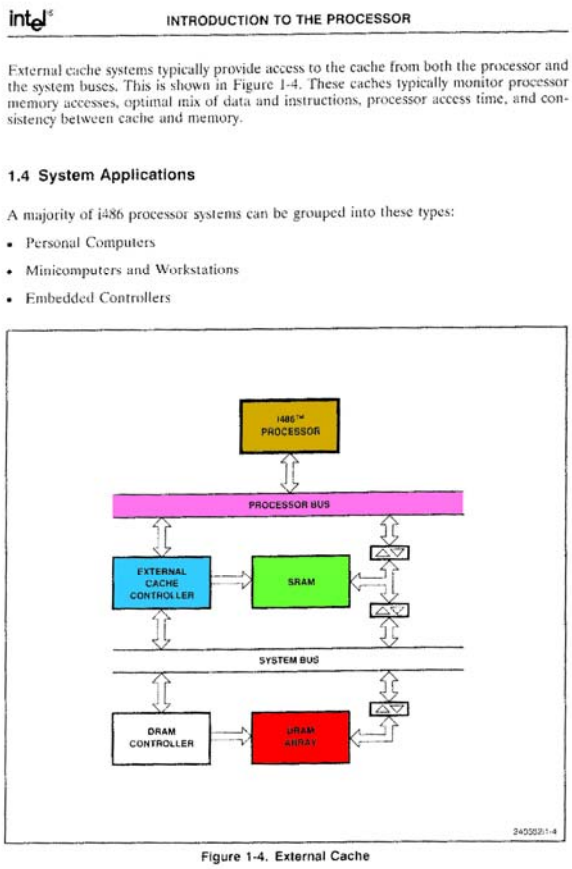


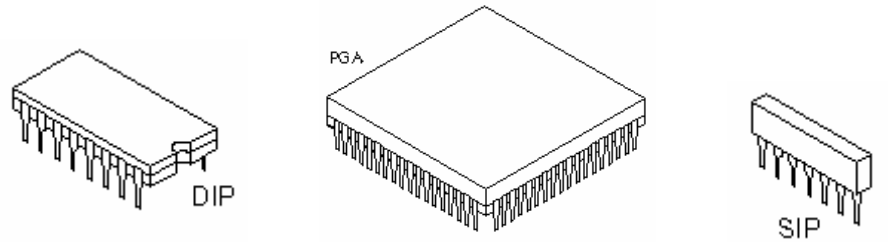
Figure 1-4. External Cache

A cache that is "external" to the CPU is located on a different semiconductor chip than the CPU. (*See id.* at 1-8.) Figure 1-4 from the 486 manual shows how an external cache chip (labeled "SRAM" and in green) and a cache controller chip (in blue) could be connected to the 486 CPU chip (in gold). (*Id.* at 1-12.) As shown in Figure 1-4, the various chips are connected to each other via a "bus," which is a group of conductors that, unlike a point-to-point connection, can permit communication among several devices. (*See id.* at 3-1.) The processor bus (in purple) depicted in Figure 1-4 is also shown in Figure 2-1 and connects the CPU chip to other devices on other chips (not shown). (*Id.*)

The Chan patents also illustrate the connection of an external cache chip (labeled 72A, 72B, 72C and 72D in Figure 7 and 72 in Figure 32) and an external controller chip (labeled 70 in Figures 7 and 32) to a 486 CPU chip (labeled 60). Patent Figures 7 and 32 provide an overall

system-level view of the connection. Figure 13 illustrates in more detail the connection between specific pins on the cache memory chip and specific pins on the 486 CPU chip.

Semiconductor chips come in a variety of packages, a few of which are illustrated below.[10] The chips have terminal pins or "pins" that are used as ports for inputting or outputting signals such as data. The pins, shown at the bottom of each figure below, are connected to a bus of the type shown in Figure 1-4 above.



As described below, the prosecution history, specification, and claims make clear that the '709 and '241 claims are directed to a cache chip that is external to the CPU.

[10] The three most common types of chip packages are DIPs (Dual In-line Packages), which have anywhere from 8 to 40 pins evenly divided in two rows, PGAs (Pin-Grid Arrays), in which the pins are arranged in concentric squares, and SIPS (Single In-line Packages), which have just one row of pins in a straight line like a comb.

II. THE CHAN PATENTS

A. Overview of the '709 Patent

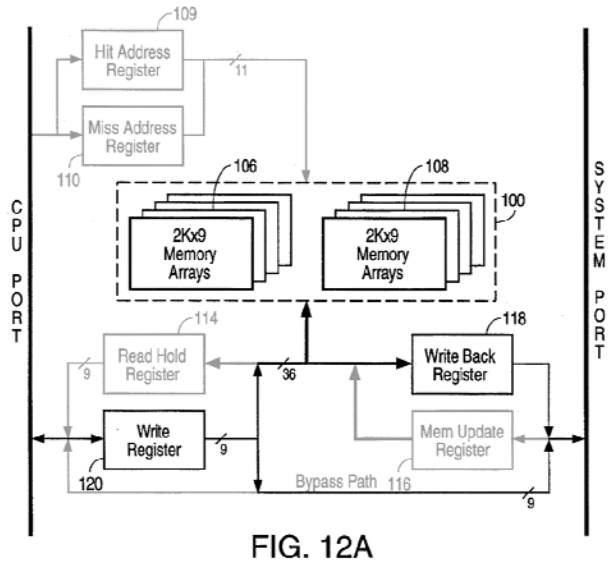


FIG. 12A

1. A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a memory write register for buffering first data received from said host port and selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port, said memory write register being coupled between said host port and said random access memory and between said host port and said system port; and

a write back register for holding second data received from said random access memory and selectively providing the second data to said system port, said write back register being coupled between said random access memory and said system port;

wherein the buffering and selective providing of the first data to said random access memory and the holding and selective providing of the second data to said system port allows memory accesses at said host port to be decoupled from memory accesses at said system port.

Claim 1 of the '709 patent is directed to a cache memory apparatus. As described in the Chan specification, and as demonstrated by the prosecution history, the claimed "cache memory apparatus" is external to the CPU chip. That is, the cache memory apparatus is itself a chip. As shown in Figure 12A (with structure in claim 1 emphasized), the cache chip is connected to the CPU via a "CPU port," which is called a host port in claim 1, and to the system memory via a "system port." Thus, the host and system ports supply the pins connecting the cache chip to the processor bus and system bus described above in Figure 1-4 in connection with the 486 processor.[11]

The '709 cache chip has a memory write register 120 that receives data from the CPU host port and then can selectively provide the data to one of (i) the random access memory 100,[12]

[11] *See supra* Part I.B

[12] An example of this action would be a "cache write hit" in a "write-back cache," as described in Part I.A.

(ii) the system port,[13] and (iii) both the random access memory and system port.[14] ('709 at 4:9-20; 32:36-48.) As discussed above, because the system memory is slower than the CPU, the memory write register can temporarily hold or buffer the data, which allows the CPU to perform other operations while the memory write register completes the write to system memory. (*See id.* at 32:36-48 (noting "zero wait states" needed).) The cache chip also has a write back register 118 for holding data that is received from the random access memory 100. (*Id*. at 10:27-30.) The write back register 118 selectively provides this data to the system port. (*Id*. at 33:12-16.) That is, depending on certain conditions present at the time, the write back register either (i) provides or (ii) does not provide the data to the system port.[15] (*Id*.)

[13] An example of this action would be where the CPU wants to write to a "non-cacheable address." That is, for some reason the computer is configured so that certain address locations in main memory are not allowed to be replicated in the cache.

[14] An example of this action would be a cache write hit in a write-through cache, where every cache write causes a write to system memory, as described in Part I.A.

[15] As described in Part I.A, if the data evicted from the cache RAM array is "dirty," the data must be written back to system memory. If the data evicted is not dirty, the data is not written back (i.e., not "provided") to system memory.

B. Overview of the '241 Patent

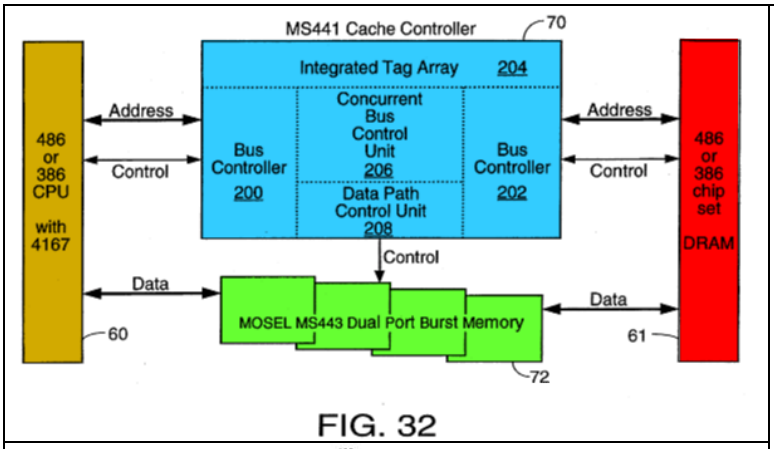


FIG. 32

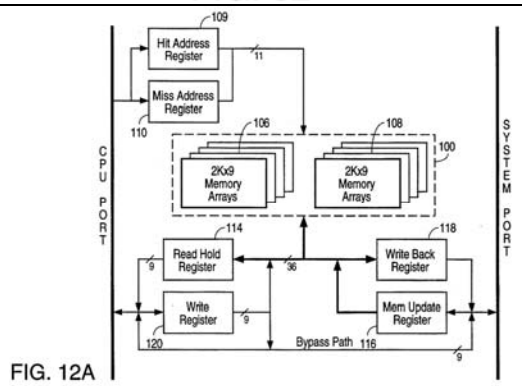


FIG. 12A

1. A computer system comprising:

a host processor having a host address bus and a host data bus;

a system memory having storage locations addressable by said host processor, a system address bus and a system data bus;

a dual port cache memory having

a system port connected to said system data bus and

a host port connected to said host data bus, said dual port cache memory comprising

cache storage locations dynamically associable with said storage locations of said system memory and

a plurality of registers coupling said cache storage locations to said host port and said system port,

wherein a data path between said host data bus and said system data bus is operably decoupled

by buffering and selective provision of data to and from said cache storage locations by said plurality of registers

so as to allow concurrent transfer of data to and from said dual port cache memory; and

a cache controller connected to said dual port cache memory, said cache controller having

a first port connected to said host address bus and

a second port connected to said system address bus

such that said dual port cache memory and said cache controller are connected in parallel between said host processor and said system memory.

The '241 patent is directed to a "computer system" comprising (1) a host processor, (2) a system memory, (3) a cache controller, and (4) a dual port cache memory.[16] The specification and the prosecution history of both the '709 and '241 patents clearly state that the claimed "cache controller" and "dual port cache memory" are both stand-alone chips that are external to the host processor (*i.e.*, CPU) chip.[17]

Figure 32 is a block diagram of the '241 system and shows how the cache controller chip ("MS441 Cache Controller") and dual port cache memory chip ("MS443 Dual Port Burst Memory") connect to the host processor ("486 or 386 CPU") and system memory ("DRAM").

[16] Independent claims 1, 15, and 16 are directed to a computer system, while independent claim 10 is directed to a "method for operating a memory cache apparatus."

[17] *See infra* Part III.

In claim 1 of the '241 patent, the dual port cache memory chip has the same "host port" and "system port" as in the '709 patent; these ports connect to the data buses that connect to the CPU (in gold) and the system memory (in red). In place of the various registers shown in Figure 12A, claim 1 recites "a plurality of registers" that are within the cache memory chip. In the '241 patent, both CPU and system memory connect to ports on the cache controller chip via an address bus.

III. THE CHAN INTRINSIC RECORD

Claim construction should not be done in a vacuum. *Phillips v. AWH Corp.,* 415 F.3d 1303, 1313 (Fed. Cir. 2005). Rather, claim construction must be based on the context of the intrinsic evidence, including the specification, claims, drawings, and the prosecution history. *Id.* at 1313-17. The specification is "the single best guide" to the meaning of the claims, and it alone is "usually dispositive." *Id*. at 1315. Where the preferred embodiment in the specification is described as the invention itself, the claims are not entitled to a broader scope than the embodiment. *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005).

A. The Prosecution History Demonstrates That The Chan Patents Are Directed To An External Cache

1. The Specification Of The '709 And '241 Patents Was Copied From MOSEL's Product Literature Describing An External Cache

The inventor of the two Chan patents, Albert K. Chan, worked at Intel Corporation as a design engineer. Intel Corporation sold two widely-used microprocessors, the 80386 ("386") and 80486 ("486"), the latter of which was discussed above. After leaving Intel and joining MOS Electronics Corp. ("MOSEL"), which was the original assignee of the Chan patents, Mr. Chan allegedly developed a cache memory chip called the MS82C443 and a cache controller chip called the MS82C441. As reflected in their data sheets, the MOSEL chips were specifically designed to work with Intel's 386 and 486 chips and as such, both are external chips.

(*See* Ex. 1.)[18]

The specification for the '709 and '241 patents was largely copied from MOSEL product literature. In fact, when the original patent application from which both patents claim priority was filed, instead of using his own words to describe his invention, Chan simply attached a 26-page MOSEL cache chip specification and a 50-page MOSEL Burst RAM architecture specification. (*See* Ex. 4; 5.) After the Patent Office rejected all the claims, Chan filed the '709 application and added to the specification by copying wholesale parts of additional MOSEL documents. For example, Figures 5, 7, 9, 10, 12b, and 13 through 31 and Table II (*see* '709 at col. 29-32) are taken verbatim from the MOSEL MS82C443 Burst-RAM datasheet. (*See* Ex. 2.) As demonstrated below, both the prosecution history and patent specification reaffirm that the '709 and '241 patents were intended to patent the specific MOSEL chips that Mr. Chan developed to work with the two Intel CPU chips. Because those chips are external, the claims in the '709 and '241 patents are limited to an external chip.

2. The '709 Claims Were Amended Four Times And Incorporated Limitations From The MOSEL Cache Chip Each Time

During prosecution of the '709 patent, Chan attempted to claim something much broader than the particular cache chip he developed, but the Examiner repeatedly rejected the claims. (*See* Ex. 8-11.) After the claims had been rejected twice and Chan had narrowed his claims twice (*see* Ex. 12-13), in the third office action, the Examiner stated:

> Note also that the mere labeling of a register (such as an "update" or "miss (hit)" register) without a recitation of its function or operation does not render the claimed invention patentably distinct.

[18] The MOSEL data sheets note certain "on chip" features and provide a "pinout" that lists the signals for the various pins for connection to other chips.

(Ex. 10 at 8.) After Chan narrowed the claims for a third time (*see* Ex. 14), the Examiner again rejected all the claims, adding:

> Applicant has not adequately addressed the explanation provided by the Examiner of how the claimed "system port," "host port," "input registers," and "output registers" are met by the references. Again note that the mere labeling of a register (such as an "update" register) without a clear recitation of its function and operation does not render the claimed invention patentably distinct. The functional language "the writing…and…providing of data…'allowing' the host port to be decoupled" is not sufficient to patentably define the claimed invention over the prior art.

(Ex. 11 at 6.) In response to this rejection, Chan amended the claims to finally add enough structural and functional limitations describing how his invention worked (s*ee* Ex. 15) and the Examiner allowed the claims. As support for these additional limitations, Chan cited to the text that is found in the '709 specification at 32:37-34:2 and 39:26-40:7. (*Id.* at 13-14.)

3. The '241 Claims Were Amended Five Times And Incorporated Limitations From The MOSEL Chips Each

Including the original priority application and the continuation application, the '241 claims were rejected five times (*see* Ex. 8; 16-19), and after each rejection, Chan narrowed the claims. (*See* Ex. 20-24.) Although the '709 and '241 patents were examined by different Examiners, the '241 Examiner also made a statement about the broad claims that Chan was attempting to patent:

> A cache memory is a fast memory element and without specific caching details appearing in the claims, any memory element, especially one designated by the reference as a cache is considered equivalent to a cache memory unless specific details of the claimed cache are present in the claims. … As to the input registers, the holding registers and output registers are taught to the extent claimed.

(Ex. 19 at 2 (emphasis added).)

The '241 claims, like the '709 claims, also were not allowed until Chan narrowed his claims to (as the applicant admitted) "obtain a more appropriate scope of coverage." (Ex. 24, Paper 25 at 7.) As support for adding the "data path," "decoupled," and "plurality of registers"

limitations, for example, Chan cited to the text that is found in the '709 specification at 3:64 to 4:2; 41:25-43; and 43:20-32. (*See* Ex. 21 at 8-9.)

4. During Prosecution, The '709 And '241 Claims Were Limited To An External Cache Chip

In narrowing the claims to patentably define over the prior art and obtain his patents, Chan repeatedly cited portions of the specification copied from product documentation describing the MOSEL external cache chip. As support for adding the "write back register" limitation, Chan cited to the text from 32:37 to 34:2 (Ex. 15 at 13-14), which was copied verbatim from pages 14-16 of the data sheet for the MOSEL MS82C443 Burst-RAM cache chip data sheet. (Ex. 2.) Similarly, as support for the "selectively providing" limitation that was added, Chan cited to the text from 39:26 to 40:7 (Ex. 15 at 13-14) and that language comes directly from pages 24-28 of the same data sheet. (*See* Ex. 2.) In fact, if one were to replace "MS82C443" in the MOSEL data sheet with "cache memory 72," the language exactly tracks the '709 passage. (*See id.*)

The language Chan cited as support for adding the "data path," "decoupled," and "plurality of registers" limitations in the '241 prosecution similarly demonstrates that the invention is an external cache chip. The text at 41:25-43 and 43:20-32 is copied from the MS82C443 external cache data sheet (*see* Ex. 2 at 28, 35.) and the text at 3:64 to 4:2, although not copied verbatim, was paraphrased from the Description of that chip on the first page of the data sheet. (*See id.)*

Thus, in the prosecutions of both the '709 and '241 patents, when forced by the Patent Office to add limitations directed to the precise structure and operation of his invention, Chan relied exclusively on the MOSEL external cache chip. These facts alone demonstrate that Chan's invention is limited to an external cache (but there is more - *see, e.g.,* Sections III.B. and

III.C below).

The prosecution history is consulted during claim construction to determine what the inventor understood the invention to be and, more importantly, "whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see also Chimie*, 402 F.3d at 1384 ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'"). Here, Chan understood his invention to be an external cache chip, and any construction other than an external cache chip must be excluded.

B. The Specification Also Demonstrates That The Claims Of The Chan Patents Are Directed To An External Cache

1. The Specification Of The '709 And '241 Patents Consistently Refers To A Cache External To The CPU As The Invention

Throughout the specification, Chan consistently describes a cache memory chip that is external to the CPU as "the invention." For example, the "Description of the Embodiments" section notes that "a diagram of the burst RAM cache memory chip in accordance with the invention is shown." ('709 at 7:7-15 (emphasis added).)[19] In addition, Chan repeatedly refers to the "present invention," as directed to cache memory consisting of four "burst RAM cache memory IC's." ('709 at 6:49-55.) As noted above, "IC" is shorthand for an "integrated circuit," or semiconductor chip, indicating that the invention is an external cache.

The patent figures also provide telling evidence that the '709 and '241 patents are limited to the an external cache chip. Figure 7, described by Chan as "a block diagram of a computer system in accordance with the present invention based on the model 80486 microprocessor," is lifted from the MS82C443 datasheet (Ex. 2), and depicts a cache chip that is external to the CPU.

[19] *See also* '709 at 72:59-61.

('709 at 4:52-54 (emphasis added).) Likewise, Figures 12A, 12B, 13 and 14 are copied directly from two MOSEL MS443 Dual Port Burst Memory data sheets, (*see* Ex. 1 at 9-5; Ex. 2 at 13, 39, 40), and the specification describes these figures as "the invention":

> FIGS. 12A and 12B are shown to simplify the conceptual architecture of the burst RAM cache memory 72 in accordance with the invention. The architecture shown in FIGS. 12A and 12B corresponds to that of FIGS. 8A-8C, and includes hit address register 109, miss address register 110, RAM array section 100, read hold register set 114, memory update register set 116, write back register set 118, and write register 120. The generalized diagrams of FIGS. 12A and 12B may be referred to for simplifying the descriptions of the cache memory 72 contained herein.
>
> The burst RAM cache memory 72 and controller 70, in accordance with the invention, control the paths of data in response to various control signals. These signals, along with the terminal pins of cache memory 72 and controller 70 from which and to which they are provided, are listed below in Tables I and II with a brief description of their purposes. In addition, FIGS. 13 and 14 illustrate the system and host interface connection pins for an 80486 computer system incorporating a cache memory 72 and controller 70 in accordance with the invention.

('709 at 10:37-56 (emphasis added).) In addition, the four cache chips in Figure 13 are labeled "MS82C443." And, in Figure 14, the cache controller chip is labeled "441" (shorthand for the MOSEL MS82C441) and the cache chips are labeled "443's" (shorthand for the MOSEL MS 82C443). Further, Figure 32, which is a system diagram showing the cache controller chip and cache memory chip connected to a CPU and to system memory, came directly from the MOSEL MS 441 Cache Controller data sheet and also labels the controller as "MS441" and the cache as "MOSEL MS443 Dual Port Burst Memory." (Ex. 1 at 9-3.)

Additionally, the Chan specification details how the cache chip and cache controller chip interact with the internal cache of the 486. For example, at various places the Chan specification notes that "[t]he great majority of operations will occur with the 486 CPU internal cache turned on" ('709 at 49:46-49), "[i]f the 486 CPU internal cache is enabled and a hit occurs" (*id.* at 56:61-63), and "[t]his will prevent the corresponding data from being cached inside the i486

CPU internal cache." (*Id.* at 57:24-25). If the Chan patents were directed to an internal cache, there would be no need to describe these operations.

Because the '709 and '241 patents consistently refer to the external cache embodiment as "the invention," the claims are limited to a cache chip that is external to the processor. *See Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005).

2. The Chan Specification Disclaimed An Internal Cache

Where the specification describes a particular structure as inferior or points out its disadvantages vis-à-vis the invention, the patentee disclaims that structure. *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343 (Fed. Cir. 2001). In the "Background of the Invention" section, the Chan specification describes the operation of the Intel 486 internal cache to illustrate the drawback of that type of cache. ('709 at 3:16-33.) By pointing out that "additional data cycles" are needed to fill an internal cache, the '709 and '241 patents disclaimed that structure and are limited to an external cache. *See SciMed*, 242 F.3d. at 1343.

The facts in this case are analogous to *Alloc, Inc. v. ITC*, 342 F.3d 1361, 1370 (Fed. Cir. 2003). The patents-in-suit in *Alloc* were directed to floor panels, and the Federal Circuit considered whether the claims should be interpreted to require "play," (*i.e.*, displacement between panels) even though none recited that limitation. *Id*. at 1368. The court noted that in some instances the specification may indicate that the claims have been limited to a subset of possible embodiments, and in others the specification may "suggest[] that the very character of the invention requires [a] limitation be a part of every embodiment." *Id*. at 1370.

In examining the specification, the court reasoned that not only did all the embodiments either disclose or imply that play was required, but that in referring to these embodiments as "the invention," the specification taught that the invention as a whole required "play." *Id*. at 1369.

As further evidence, the court noted that "all the figures … in the asserted patents imply play, or, as in the case of Figure 1b, expressly disclose play." *Id*. at 1370. In addition, the court noted that the specification for the patents-in-suit criticized prior art floor systems not having play. *Id*. In affirming a construction requiring the claims to have structure that allowed "play," the Federal Circuit reasoned that "where the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims." *Id*. at 1370.

The facts here present an even more compelling case than in *Alloc*. All of the embodiments in the Chan specification and each of the figures (excepting those marked "prior art") expressly disclose an external cache chip. Where an internal cache is discussed, Chan notes that it is part of the prior art, and uses it to illustrate the drawback of that particular structure. Because all of the embodiments in the Chan specification teach an external cache chip, coupled with the fact that these embodiments are consistently referred to as "the invention," the '709 and '241 claims should be limited to an external cache. As in *Alloc*, the very character of Chan's invention requires that limitation be a part of every embodiment. *See id.* at 1370.

C. Construing The Chan Patents To Be Limited To An External Cache Is Not Impermissibly Importing A Limitation From The Specification

Notwithstanding the foregoing extensive intrinsic evidence that the Chan patent claims describe a cache chip that is external to the processor, Freescale expect ProMOS to argue that Freescale is improperly attempting to read limitations from the specification into the claims. Not so. The Federal Circuit has repeatedly held that a patentee may not disclose an invention narrowly, yet be entitled to a broad scope of claims. Where, as here, the inventor has "described [his] invention narrowly and with specificity," the patent claims will not be construed as if the invention had instead been broadly disclosed. *Cultor Corp. v. A.E. Staley Mfg. Co.*, 224 F.3d

1328, 1331 (Fed. Cir. 2000); *see also Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) ("We cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its inventions and represented to the PTO.").

Based on the specification, drawings, and prosecution history, a person of ordinary skill in the art would draw the "inescapable conclusion" that the '709 and '241 patents are limited to an external cache. *See Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1374 (Fed. Cir. 2005). In fact, the patents do not contain any written description that would permit them to be construed in any other way.

IV. CHAN CLAIM CONSTRUCTIONS

The Federal Circuit has recently reaffirmed the importance of the patent specification in construing the claims. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1313.

A. "cache memory apparatus" / "cache memory" - '709 claims 1, 13, 17, 22 and '241 claims 1, 15, 16

Freescale	ProMOS
a memory chip that is external to the CPU chip	"cache memory apparatus" does not need construction. "cache memory" = a small block of high speed memory associated with a computer processor/microprocessor (CPU)

Freescale's construction properly recognizes that the '709 and '241 inventions comprise a memory device that is external to the CPU chip and is itself a chip. ProMOS's construction provides no guidance as to what "associated with a computer processor/microprocessor (CPU)" means. ProMOS's use of this undefined "associated with" term would stretch the claims far beyond the invention in an attempt to cover caches that are internal to the CPU chip. ProMOS's construction is contradicted by the prosecution history and specification, and should be rejected.

1. Preamble Claim Terms Should Be Construed Where, As In This Case, They Give Meaning To The Claimed Invention

Even though "cache memory apparatus" is in the preamble of claims 1, 13, 17 and 22 of the '709 patent, it should be construed. The preamble term here serves to limit the claims to a cache memory apparatus. The preamble, which states the purpose and context of the invention, constitutes a limitation of each claim in view of the overall form of the claim itself, and the invention as described in the specification and illuminated in the prosecution history. *See Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1572-73 (Fed. Cir. 1996).

First, the structure of the claims themselves indicates that the drafter intended the preamble to be part of the definition for the claimed invention, and it should be given that effect. *See, e.g., Bell Commc'n Research, Inc. v. Vitalink Comm. Corp.*, 55 F.3d 615, 620 (Fed. Cir. 2007). If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is necessary to give life, meaning, and vitality to the claim, then the claim preamble should be construed as if in the balance of the claim. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999) (quotations omitted).

Each relevant Chan claim includes terms that require the cache memory apparatus preamble to provide meaning. For example, the terms "host port" and "system port" of claim 1 of the '709 patent are unclear without proper context. A port is "an access point for data entry or exit."[20] Without context, one would not know the device for which these ports provided an access point. The preamble term "cache memory apparatus" places host port and system port in proper context, i.e., host port and system port of the cache memory apparatus. The claim preamble "cache memory apparatus" thus is necessary to give life, meaning, and vitality to the

[20] Ex. 26 *IBM Dictionary of Computing* 517 (10th ed. 1993).

claims and constitutes a claim limitation.

Second, the Chan specification indicates that the preamble was intended to be a means of defining the invention, which also mandates that it be given its intended effect. *See, e.g.*, *Rockwell Int'l Corp. v. United States*, 147 F.3d 1358, 1362 (Fed. Cir. 1998); *Bell Commc'n*, 55 F.3d at 621. Specifically, the specification defines the invention as directed to a cache memory chip: "the burst RAM *cache memory chip* in accordance with the invention" ('709 at 7:12-13, 72:60-61.) The preamble term "cache memory apparatus" is the claim language that equates the claims to a cache memory chip. The specification, therefore, leads to the conclusion that "the cache memory apparatus" preamble term does define the invention and constitutes a limitation.

Third, clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art requires the preamble to be a claim limitation because it indicates the inventor's intent to use of the preamble to define, in part, the claimed invention. *See generally Applied Materials*, 98 F.3d at 1572-73. During prosecution, Chan consistently distinguished prior art by stating that his invention was directed to a cache memory having particular structure and functionality. (*See* Ex. 13 at 9-12; 24 at 9-13.) Additionally, when confronted with rejections Chan cited to specification passages that were copied directly from MOSEL cache memory chip product literature as support for newly added claim terms. *See supra* Part III.A.4.

The claims, specification, and prosecution history thus all demonstrate that the "cache memory apparatus" helps define the Chan inventions and should be treated as a claim limitation that limits each relevant claim to a cache memory apparatus.

2. The Chan Specification Disclaimed A Cache Memory That Is Internal To A Processor Chip

When a patent applicant defines his invention by describing in the specification the differences between his invention and the prior art, the claims, as a matter of law, may not be

construed to cover the prior art that was distinguished. *See, e.g., Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1378-79 (Fed. Cir. 1998) ("[B]y distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover."). In his specification, Chan distinguished his invention from the prior art internal cache systems.

In the Background of the Invention section, Chan described the prior art as including a cache memory that was internal to a CPU chip: "The model 80486 microprocessor provides a number of additional features, including an internal cache." ('709, 2:25-29).

Chan next distinguished the invention from the "internal cache" by describing his invention as an external cache chip: "burst RAM *cache memory chip* in accordance with the invention" ('709 at 7:12-13; 72:60-61). Chan further distinguished his cache memory chip invention by describing his invention as having terminal or interface pins (*see, e.g.,* '709 at 10:50) to interface with the interface pins of the CPU chip,[21] via a data bus that was also external to the CPU chip.[22] Chan relied on these differences to obtain the patents-in-suit from the Patent Office and, consequently, disclaimed a cache that is internal to a processor.

3. Chan Described The Invention As Being Directed To A Memory Chip That Is External To The CPU Chip

Throughout the specification, the Chan patents consistently described the invention as a cache memory chip that is external to the CPU chip. The "invention," Chan explains, is directed to cache memory[23] consisting of four cache memory chips.[24] When describing the operation of

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[21] *See, e.g.*, '709 at 4:62-64 ("FIG. 13 is a diagram illustrating the host interface between the 486 microprocessor and cache controller 70 and cache memory 72.").

[22] '709 at 6:58-60 ("data is transferred between the microprocessor 60 . . . and the hot port HP of the cache memory 72 over the local data bus 26.").

[23] *See, e.g.*, '709 at 10:38-39 ("burst RAM cache memory 72 in accordance with the invention."); '709 at 10:47-48 ("The burst RAM cache memory 72 and controller 70, in accordance with the invention.")

one or more of the burst RAM cache memory chips, Chan describes the invention as burst RAM cache memory. ('709 at 6:49-50.) When specifically limiting the description to a single cache memory chip, the Chan specification consistently defines the invention as the burst RAM cache memory chip.[25]

Such statements directed to the invention as a whole, and such consistent description of all embodiments of that invention, requires the claim language to be limited to the invention as described.[26] Statements like Chan's directed to the "invention" are "not limited to describing a preferred embodiment, but more broadly describe the overall invention[ ] of [the] patent[ ]." *Microsoft Corp.*, 357 F.3d at 1348. "[W]here the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims." *Alloc, Inc.*, 342 F.3d at 1370. Thus, Chan's description of the invention as a "cache memory chip" is limiting.

4. An Object Of The Invention Cannot Be Achieved Unless The "Cache Memory Apparatus" Is Construed As An External Cache

An important advantage achieved through the invention is that "[d]ecoupled buses avoids

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(. . . continued)

[24] *See, e.g.*, '709 at 7:12-13 ("The cache memory 72 consists of four substantially identical byte-wide burst RAM memory ICs 72A, 72B, 72C and 72D to support the 32-bit (4-byte) bus system.")

[25] '709 patent at 7:12-13; 72:60-61 ("the burst RAM cache memory chip in accordance with the invention"); 8:33-34 ("the cache memory chip of FIGS. 8A-8C.")

[26] *See, e.g., Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1306 (Fed. Cir. 2005) ("Although the written description does not define 'operatively,' it consistently describes the purpose of the device to be for posterior stabilization."); *see also Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1379 (Fed. Cir. 2006) ("Thus, the specification of the '714 patent consistently, and without exception, describes adjustment that occurs during operation of the de-header system. The district court's construction of "adjustable," which includes a structure that requires dismantling of the valve to perform the adjustment, finds no support in the overall context of the '714 patent specification.").

the necessity to redesign the system memory subsystem every time the processor module is upgraded." ('709 at 73:44-46).[27]

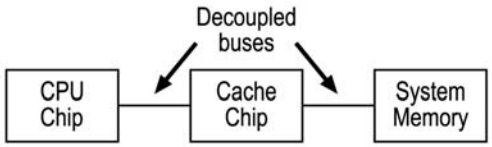

Fig. 1

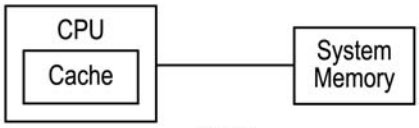

Fig. 2

As shown in Figure 1 above, an external cache chip is between the CPU chip and system memory. If, as suggested in the Chan specification, the processor is upgraded to a faster model, the cache will accommodate changes in the CPU speed and "the system memory need not be redesigned to run at the same speed as the [new] processor." ('709 at 73:48-49.) Because the external cache chip is connected to the CPU, that chip, and not the system memory, needs to accommodate changes to the speed of the CPU.

Achieving this advantage is not possible, however, when the cache is internal to the CPU. As illustrated in Figure 2, when the cache is internal to the CPU, the system memory does need to accommodate speed changes to the CPU because the system memory connects directly to it.

When advantages of the invention are unachievable without a particular limitation, the claims should be construed to include that limitation. *Nystrom v. TREX Co.*, 424 F.3d 1136, 1143-45 (Fed. Cir. 2005) (limiting "board" to only those boards cut from logs because stated advantage of reducing the amount of scrap in the outermost boards cut from a log was unachievable unless the board was cut from a log).

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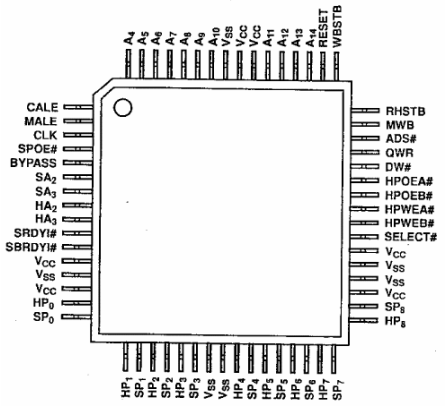
[27] *See also* '709 at 3:64-67 ("The cache memory system of the present invention decouples the main memory subsystem from the host data bus [(i.e., the data bus between the CPU and the cache memory)], so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed . . .").

5. MOSEL's Description Of Chan's Patented Product Illustrates That The Cache Memory Is A Chip That Is External To The Processor

The product literature upon which the Chan patent specification was derived specifically discloses in schematic form that Chan's burst RAM cache memory apparatus is a separate chip that is external to the processor chip:



Section 1. MS82C443 Pinout (Top View)

Depicted above is a figure of the patented cache memory chip from the product data sheet from which much of the text and figures from the Chan patents were copied. (*See* Ex. 1.) The above figure depicts a chip containing a number of labeled terminal or interface pins for the patented cache memory chip. The labels on the terminal pins depicted in this figure match up with and are more fully described in Table II of the Chan specification (beginning at Col. 29 of the '709 patent). This figure specifically shows the host port (HP) pins and the system port (SP) pins. This is a further illustration that Chan patented a cache memory chip that was external to the CPU processor chip to which it ultimately will be connected.

For all of the reasons discussed above, "cache memory" and "cache memory apparatus" should be construed to be a chip that is external to the CPU chip.

B. "host port" and "system port" - '709 claims 1, 13, 17, 22 and '241 claims 1, 10, 16

Freescale	ProMOS
host port	
a set of pins on the cache memory chip used for the input and output of data over the host data bus	interface between a cache memory and a host processor or host data bus

system port	
a set of pins on the cache memory chip used for the input and output of data over the system data bus	interface between a cache memory and a system memory or system data bus

A port is "an access point for data entry or exit."[28] The only structure described in the specification for the host and system ports are pins. Freescale's construction is consistent with the specification, prosecution history, and with the generally-understood meaning of "port."

ProMOS's proposed construction again ignores the fact that these structures represent the connection from one chip to another, instead casting "host port" and "system port" as merely some vague and undefined "interface." ProMOS's construction is an attempt to read out the host and system port limitations in order to try to accuse an interface that is internal to a chip.

1. The Specification Is Clear That The Host Port And System Port Are Pins On The Cache Memory Chip

The Chan specification describes the cache memory chip of the invention as having two ports as access points for data entry and exit to the chip, a host port and a system port:

> The burst RAM cache memory chip is provided with a 9-bit (including parity) host port HP 113 which is connected to the local (host) data bus (bus 26 of FIGS. 6 and 7) through a 9-bit line. Each burst RAM chip is also provided with a 9-bit (including parity) system port SP 112 which transfers an appropriate byte of information between the system data bus (bus 34 of FIGS. 6 and 7) through its 9-signal line." ('709 at 9:48-55.)

The Chan specification further describes, for example through Table II, that the host and data ports are pins on the cache memory chip:[29]

> [T]he terminal pins of cache memory 72 and controller 70 . . . are listed below in Tables I and II with a brief description of their purposes" ('709 at 10:50-51)

HP<8:0>	Inputs/ Outputs	Byte-wide (with parity) data input/output to and from the host
SP<8:0>	Inputs/ Outputs	Byte-wide (with parity) data input/ output to and from main memory.

[28] Ex. 26, *IBM Dictionary of Computing* 517 (10th ed. 1993)

[29] Chips have pins that are used as ports. *See* discussion of chips *supra* at Part I.B.

The Chan specifications further instructs that "FIGS. 13 and 14 illustrate the *system and host interface connection pins* for an 80486 computer system incorporating a cache memory 72 and controller 70 *in accordance with the invention*." ('709 at 10:53-56)

The pins on the cache memory chip are the only structure described in the patent specification for the host and system ports. The product literature from which the Chan patent specification was derived also shows that the host port HP and the system port SP are specific pins on the cache memory chip (as illustrated in the figure in Part IV.A.5, *supra*). The Federal Circuit made clear in *Phillips* that the meaning of claim terms should be consistent with the context of its use in the intrinsic record. 415 F.3d at 1312-17; *Nystrom*, 424 F.3d at 1145 ("[I]n the absence of something in the written description and/or prosecution history to provide explicit or implicit notice to the public – *i.e.*, those of ordinary skill in the art – that the inventor intended a disputed term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise or other extrinsic source.").[30] Freescale's proposed construction of host port and system port should therefore be adopted.

C. "dual port cache memory" - '241 claims 1, 15 and 16

Freescale	ProMOS
a cache memory chip having a host port and a system port.	a cache memory that has that has two interfaces

Because the Chan specification describes the cache memory chip as having precisely two ports, a host port and a system port, "dual port cache memory" must be construed, consistent with the patent specification, to be a cache memory chip having the two disclosed ports, the host

[30] *See also MicroStrategy, Inc. v. Bus. Objects SA*, 429 F.3d 1344, 1351 (Fed. Cir. 2005) (though the literal language of the claims did not recite multiple styles, the context required more than one); *Tap Pharm. Prods., Inc. v. Owl Pharms.*, 419 F.3d 1346, 1354 (Fed. Cir. 2005) (context required a drug-retaining substance, though the claims did not recite one).

port and the system port. ProMOS's proposed construction, which includes "two interfaces" and fails to include a cache memory chip presumably is offered to broaden the claims to cover the internal caches that, as demonstrated above, were expressly disclaimed by Chan in order to obtain these patents. The meaning of claim terms should be consistent with the context of their use in the intrinsic record. *Phillips*, 415 F.3d at 1312-17. Freescale's construction should be adopted.

D. "cache controller" / "controller" - '241 claims 1, 15 and 16

Freescale	ProMOS
a chip that controls a cache memory chip	circuitry that controls the transfer of data or other information to and from cache memory

In addition to the cache memory chip, the Chan specification describes the invention as including a cache controller chip that is external to the microprocessor. For example, the specification describes that the "controller 70, in accordance with the invention" "presents a very 486 CPU-like interface to system logic. The great majority of *system interface pins* [on the controller 70] have the same name and functionality as their 486 CPU counterparts. Because of these features, designing the controller 70 into a system is very straightforward. Glue logic to design in the [controller] chipset is minimal." ('709 at 50:46-51.) In another example, the Chan specification describes that "[o]n the system side, the controller 70 has an [almost] identical *list of pins* as does the i486 CPU." ('709 at 50:61-62.) Because the specification consistently describes the cache controller as a device having interface pins, it is a chip, which controls a cache memory.[31] ProMOS's construction, once again, fails to acknowledge that the cache controller is a separate chip. Freescale's proposed construction does, and should be adopted.

[31] It is clear that the function of the cache controller is to control a cache memory chip. *See e.g.*, '709 at 46:43-44 ("Each controller 70 will provide control for 64K byte of cache memory.".)

E. "first port" and "second port" - '241 claims 1 and 16

Freescale	ProMOS
"first port"	
pins on cache controller chip used for the input and output of address information over the host address bus	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: "a port connected to the host address bus"
"second port"	
pins on cache controller chip used for the input and output of address information over the system address bus	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: "a port connected to the system address bus"

Similar to the host and system ports on the cache memory apparatus, the first and second ports comprise certain terminal pins on the controller chip for the input and output of address information over the host address bus and the system address bus, respectively. In particular, terminal pins A(31:2) are defined in Table I as the address pins (*i.e.*, first port) that connect to the host address bus and terminal pins SA(27:2) are defined in Table I as the address pins (*i.e.*, second port) that connect to the system address bus. In addition, Figure 33 shows the controller pins. ProMOS's proposed construction ignores the fact that the ports represent connections to and from a chip. Freescale's proposed construction should be adopted.

F. "host processor" / "host" / "host microprocessor" - '241 claims 1, 10, 15, 16

Freescale	ProMOS
a single chip central processing unit (CPU)	CPU associated with one or more cache memories

The Chan specification uses the terms "host," "host processor," and "microprocessor" interchangeably to describe the 80386 and 80486 microprocessors.[32] Microprocessor has a well-known meaning in the art, i.e., a single chip central processing unit (CPU).[33] This meaning is consistent with Chan's use of these claim terms in the specification. These terms are each used to describe the two examples, the Intel 386 and 486 microprocessors. ProMOS' suggestion of "CPU associated with one or more cache memories" as a possible construction is vague and

[32] *See*, *e.g.*, '709 at 6:52 (microprocessor 60), 8:43 (CPU 60), Table I (host CPU); 73:35 (host processor 60).

[33] Ex. 27, *Microsoft Press Computer Dictionary* 307 (3d ed. 1997).

confusing (what does "associated with" mean?), and ignores the fact that all examples in the specification are of single chip CPUs.

As further evidence of the intended claim scope, claim 1 of the Chan '241 patent and Figure 32, for example, specifically demonstrate that Chan intended for the CPU chip, cache controller, and cache memory to be separate chips. All examples in the Chan specification illustrate that each of the CPU chip, cache memory, and cache controller are in separate chips; there is no support to the contrary anywhere in the intrinsic evidence. Freescale's proposed construction should be adopted.

G. "host address bus" and "host data bus"

Freescale	ProMOS
host address bus	'241 claims 1, 15, 16
A set of conductors connected to the address terminal pins of a CPU chip used to transfer memory addresses from the CPU to other components of a computer system	Bus - line or set of lines used to transfer data or other information Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.
host data bus	'241 claims 1, 15, 16
A set of conductors connected to the data terminal pins of the CPU used to transfer data to and from the CPU and other components of a computer system	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing host data.

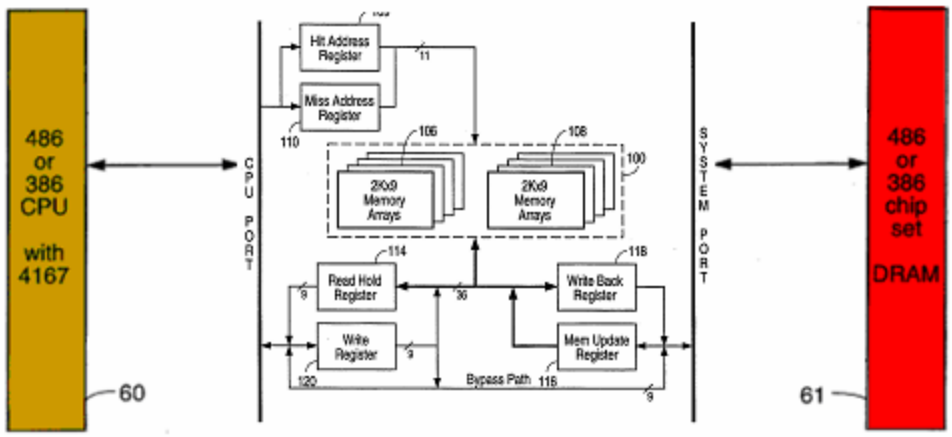
A bus is a set of conductors used to transfer data between devices.[34] The Chan specification discloses that the host address and data buses are connected to the CPU address and data pins. ('709 at 10:53-56; Figure 13.) ProMOS's proposed construction ignores the ports on the CPU chip to which these buses are connected. The context of use of these claim terms in the Chan specification mandates that Freescale's proposed construction of these terms be adopted.

[34] *See e.g.*, Ex. 26, *IBM Dictionary of Computing* 77 (10th ed. 1993) (defining "bus" as "one or more conductors used for transmitting signals or power"); Ex. 27, *Microsoft Press Computer Dictionary* 68 (3d ed. 1997) (defining bus" as "a set of hardware lines (conductors) used for data transfer among the components of a computer system"); Ex. 28, *IEEE Standard Dictionary of Electrical and Electronic Terms* 141 (5th ed. 1993) (defining "bus" as "one ore more conductors used for transmitting signals or power from one or more sources to one or more destinations").

H. "buffering" - '709 claims 1, 13 & 22 and '241 claim 1

Freescale	ProMOS
Using a storage element (e.g., memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (e.g., the CPU) to another external device (e.g. system memory) because of differences in rates of data flow or time of occurrence of events.	storing data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of data

The patent specification specifically distinguished between a "buffer" register and a "hold" register. With reference to the figure below (in which patent Figure 12A is superimposed onto Figure 32), Chan defined 1 of the 4 data registers in the cache memory apparatus (the write register 120) as a buffer register and defined the other 3 registers (114, 116 & 118) as hold registers. ('709 at 10:20-23; 32:39-42.) In defining "buffering," Chan described two modes of operation where the memory write register 120 functioned as a buffer: (1) buffered non-cacheable writes, *i.e.*, writes by the CPU 60 where data is passed to system memory 61 via a write operation at the CPU port to the write register 120 and then the write register 120, in turn, selectively provides (another claim term discussed below) that data to the system port for storage into system memory 61; and (2) buffered write-through cycles, *i.e.*, writes by the CPU 60 where data is passed to system memory 61 and the cache RAM memory arrays 100 via a write operation at the CPU port to the write register 120 and then the write register 120, in turn, selectively provides that data to the system port for storage of the data into system memory 61 and to the cache memory arrays 100. ('709 at 32:37-48.) In both cases, the memory write register 120 acts as a buffer between two devices external to the cache, the CPU 60 and system memory 61, for writes by the CPU to system memory.



In contrast, the hold registers are described as involving data transfers between the internal cache RAM arrays 100 and one external device (the CPU 60 or system memory 61) using an internal cache data register (114, 116 or 118) to temporarily hold data during the transfer operation. These data transfers do not involve data transfers between two devices external to the cache in which the cache serves as an intermediary to the transaction. To the contrary, the read hold register 114 temporarily holds data to be transferred from the cache RAM arrays 100 to the CPU 60, the write back register 118 temporarily holds data to be transferred from the cache RAM arrays 100 to system memory 61, and the memory update register 116 temporarily holds data to be transferred from system memory 61 to the cache RAM arrays 100. ('709 at 32:50-58; 33:1-11; 33:21-29.)

In addition to this "external" versus "internal" device distinction, the buffering functionality supports an important object of the invention, to accommodate "differences in the speed of the local and system buses." ('709 at 4:2-3.) Buffering is conventionally understood to involve using an intermediary temporary storage device to temporarily hold data that is waiting to be transferred from one device to another because of differences in rates of data flow or time

of occurrence of events.[35]

ProMOS's proposed construction ignores the distinction made by Chan, that buffering involves using the cache as an intermediary between two different devices that are external to the cache chip when transferring data from one of the external devices to the other. Freescale's proposed construction, therefore, should be adopted.

I. "selectively providing" - '709 Claims 1, 13, 17 and 22

Freescale	ProMOS
providing data held in a register depending on certain conditions and never providing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe the term anyway, it means: providing on a selective basis.

In both the claims and the specification, "selectively providing" is used to describe conditions under which a register provides or will never provide certain data held in the register. For example, in claim 1, the write back register 118 is for "holding second data received from said random access memory and *selectively providing* the second data to said system port." The specification describes this two-part operation (i) data that is being replaced from the cache RAM array is written to and held in the write back register, and (ii) if the data is "dirty," it is provided to system memory.[36] That is, the evicted data must be valid and dirty; if it's not, the

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[35] Ex. 26, *IBM Dictionary of Computing* 75 (10th ed. 1993) (defining "buffer" as "storage used to compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from one device to another"); Ex. 27, *Microsoft Press Computer Dictionary* 66 (3d ed. 1997) (defining "buffer" as "a region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations" and "to use a region of memory to hold data that is waiting to be transferred"); Ex. 28, *IEEE Standard Dictionary of Electrical and Electronic Terms* 135 (5th ed. 1993) (defining "buffer" as "a storage device used to compensate for a difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another.").

[36] *See, e.g.*, '709 at 33:14-16 ("This data is written back to main memory *if the replaced line contains valid and dirty data*."); *id*. at 42:29-33 ("A write-back burst sequence should occur *if the data replaced is dirty*."); *id*. at 61:64-67 (". . . for later write-back *if dirty data was present* in the replaced line.") *id*. at 70:51-53 ("*If the current line contains dirty data,* state 328 is entered wherein the contents of memory write back register set 118 are dumped to the (Continued . . .)

data is not written back (*i.e.*, "provided") to system memory.[37]

ProMOS's construction does nothing more than circularly rearrange the words of the claim and provides no guidance as to what the term actually means. ProMOS's construction also impermissibly writes out the claim term "selectively" by dodging the requirement that under certain conditions the data will never be provided. Freescale's construction is consistent with the claims and specification and should be adopted. This rationale should also be applied to the other "selectively providing" phrases at TAB 2A.

J. "selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port" - '709 Claim 1

Freescale	ProMOS
The selectively providing claim phrase means providing the first data to: [a] said random access memory and not to said system port under one set of conditions, [b] said system port and not to said random access memory under a second set of conditions, and **[c]** said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above, and ProMOS's position on "selectively providing" and "random access memory above.

Freescale's construction is straight-forward and should be adopted. Because the claim phrase uses the conjunctive term "and," instead of the disjunctive term "or," the selectively providing requirement applies to each of elements a, b, and c. This rationale should also be should also be applied to the other "selectively providing to one of [a], [b], and [c]" claim phrases listed at TAB 2B.

(. . . continued)
system port 112.") (emphases added).

37 *Id.*

K. "at the same time" - '709 Claim 13 and 22

"wherein the input data *is provided* to said random access memory from said memory write register *at the same time* that the output data *is provided* by said write back register to said system port" (709:13)	
Freescale	ProMOS
whenever input data is provided to the RAM, output data must be provided to the system port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "is provided" and "at the same time" need to be construed, these terms are clear on their face.**

The claim phrase clearly states that input data *is provided at the same time* output data *is* provided. The claim language does not allow for input data to be provided without output data being provided. The claim language is absolute. Thus, Freescale's proposed construction should be adopted. The rationale described herein should also be applied to the other "at the same time" claim phrases listed at TAB 2C.

L. Means-Plus-Function Claim Terms

- "means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port" ('709 claim 10)
- "means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port" ('709 claim 26)
- "means for masking the providing of selected ones of said words of the fetched data to said random access memory" ('709 claim 12)
- "means for masking writing of selected words of the system fetch data into said random access memory" ('709 claims 21 and 24)
- "means for masking writing of selected words of data into said random access memory" ('241 claim 26)
- "means for disabling said dual port cache memory during a local bus access cycle" ('241 claims 5 and 19)

The parties agree that each of the foregoing claim phrases are governed by 35 U.S.C. § 112, ¶ 6. *See* TAB 2D. In construing a means plus function term, the Court must identify, as a

matter of law, the function performed by the claimed "means"[38] and the structure described by the patent's specification corresponding to the "means" that performs the identified function.[39] "A structure disclosed in the specification qualifies as 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim"[40] If the patentee fails to adequately disclose the corresponding structure, the patent is invalid due to a failure to particularly point out and distinctly claim the invention as required by the second paragraph of § 112. *Biomedino*, 490 F.3d at 948.

The Chan specification does not clearly link or associate any specific structure for the functions recited in these means-plus-function claim limitations. As a result, there is no "corresponding" structure, and the claims are invalid. In attempt to save its claims, ProMOS identified the value of certain data bits as structure for the means for identifying and means for masking claim phrases. Data values or bits however are not structure. For the *means for disabling* claim phrase, ProMOS identified some undisclosed "circuitry" inside the controller as structure. This undisclosed "circuitry" does not apprise the public of the scope of the claims. All of these means-plus-function claim phrases are indefinite.

1. Non-Presumptive Means-Plus-Function Claim Terms

- "first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus" ('241 claims 4 and 18)
- "a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus" ('241 claims 4 and 18)

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[38] *Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 948 (Fed. Cir. 2007); *Chuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308 (Fed. Cir. 1998).

[39] *Chuminatta*., 145 F.3d at 1308; *Intel Corp. v. Broadcom Corp*., No. 00-796-SLR, 2003 U.S. Dist. LEXIS 2372, at*66 n.9 (D. Del. Feb. 13, 2003) (Robinson, J.) ("As a matter of law, the structure identified by the court must perform the function required by the claim.").

[40] *Default Proof Credit Card Sys. v. Home Depot U.S.A.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005).

The parties disagree regarding whether 35 USC 112 ¶ 6 is applicable to these terms. "When the word 'means' is not used in a claim term, a rebuttable presumption arises that section 112, ¶ 6 does not apply. This presumption can be rebutted, if the party advancing a means-plus-function construction demonstrates that the claim term fails to recite sufficiently definite structure or recites a function without reciting a sufficient structure for performing that function."[41] Here, the presumption should be rebutted because one skilled in the art would not know the precise structure for either a first or second control sequencer. Those terms are purely functional language without the recitation of any definite structure. Moreover, Chan did not describe any structure for performing the functions recited in these means-plus-function limitations and obviously did not clearly link or associate specific structure for the functions. Thus, there is no "corresponding" structure, and the claims are invalid under 35 U.S.C. § 112 ¶ 2.

M. Indefinite Phrase: "operations at said system port to be decoupled from said random access memory" - ('709 claims 17 and 22)

Claims 17 and 22 recite that "the holding and selective furnishing of the first output data [by the write back register] and the holding and selective providing of the second input data [by the memory update register] allows write back and memory update operations at said system port to be decoupled from said random access memory." This phrase is internally inconsistent. The memory update operation involves providing the second input data to the random access memory. The memory update operation therefore cannot be decoupled from the random access memory if it is providing data to the random access memory. Because the claim phrase is internally inconsistent, one cannot determine what falls within the scope of the claims. The result is that the claims should be invalid. *Amgen*, 314 F.3d at 1342 ("ambiguity in claim scope is at

[41] *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 422 F. Supp. 2d 446, 459 (D. Del. 2006).

the heart of the definiteness requirement").

N. Indefinite Term: "operably decoupled" ('241 claim 1)

The phrase "operably decoupled" is not a term of art and is not defined or used anywhere in the patent specification. The term "decoupled" is used in the specification and appears in a number of Chan claims. However, because "operably decoupled" and "coupled" are used in different claims, and "operably" has to mean something (it is impermissible to leave it out), "operably decoupled" cannot be construed to mean the same thing as "decoupled."[42] Moreover, the use of the term "operably decoupled" suggests that the claimed "decoupled" must mean "inoperably decoupled," whatever that means. The claim "operably decoupled" does not advise the public of the scope of the claim and is indefinite. *Id.*

O. Indefinite Register Terms: Host Input Register (Chan '241: 10, 15), First Input Register (Chan '241: 16), System Output Register (Chan '241: 10), First Output Register (Chan '241: 16), Second Output Register (Chan '241: 16), System Input Register (Chan '241: 10, 15), Second Input Register (Chan '241: 16)

The Chan specification describes the invention as having precisely 4 data register sets (no more and no less) – a memory read hold register set, a memory write back register set, a memory update register set, and a memory write register[43] – that allow the invention to achieve its stated

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[42] *Karlin Tech. Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 971-72 (Fed. Cir. 1999) ("[D]ifferent words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope.)

[43] '709 at 10:20-36 ("Referring back to FIGS. 8A-8C, the burst RAM chip data path further includes three sets of holding registers 114A-114D, 116A-116D and 118A-118D, and a memory write register 120. A memory read hold register set ("MRHREG") includes four 8-bit registers 114A-114D and is provided to support data bus burst read operations on the host data port 113. Each of the four registers 114A-114D includes an additional bit for parity. A memory write back register set ("MWBREG") includes four 8-bit (plus parity) registers 118A-118D and is provided to accommodate burst write operations on the system data port 112. A memory update register set ("memory update register set 116") includes four 8-bit (plus parity) registers 116A-116D and is provided to accommodate quad fetch miss data operations from system memory 38. Finally, memory write register 120 is an 8-bit register (Continued . . .)

goal of "decoupl[ing] the main memory subsystem from the host data bus, so as to accommodate parallel cache-hit and system memory transfer operations for increased system speed, and to hide memory write-back cycles for the microprocessor." ('709 at 3:64-4:2.)

A register is a set of bits of high-speed memory within an electronic device, used to hold data for a particular purpose.[44] It is not merely "circuitry capable of retaining data or other information, such as address information" as ProMOS suggests. ProMOS's construction is overbroad and would capture almost any circuit such as a DRAM or SRAM, which are clearly not registers.

Although the patent specification specifically defines the 4 data registers that can be used to accomplish the object of the claimed invention and which are recited in many claims, other Chan patent claims specify additional undisclosed registers. ProMOS cannot claim concepts that it never conceived and never described in its original patent application. "The written description requirement and its corollary, the new matter prohibition of 35 U.S.C. § 132, both serve to ensure that the patent applicant was in full possession of the claimed subject matter on the application filing date. When the applicant adds a claim or otherwise amends his specification after the original filing date, . . . the new claims or other added material must find support in the original specification."[45]

(. . . continued)
(plus parity) provided to accommodate scalar write operations on the host data port 113.")

[44] Ex. 27 *Microsoft Press Computer Dictionary* 402 (3d ed. 1997); Ex. 26 *IBM Dictionary of Computing* 566 (10th ed. 1993) (defining "register" as "A part of internal storage having a specified storage capacity and usually intended for a specific purpose.").

[45] *Turbocare Div. Of Demag Delaval Turbomachinery Corp. v. Gen. Elec. Co.,* 264 F.3d 1111, 1118 (Fed. Cir. 2001); *see also, Mackay Radio & Tel. Co., Inc. v. Radio Corp. of Am.,* 306 U.S. 86, 97-98 (1939) (holding that a post application amendment could not be considered in construing the scope of the claims); *see also Twin Disc, Inc., v. United States,* 231 U.S.P.Q. 417, 439-40 (Ct. Cl. 1986); *Dresser Indus., Inc. v. United States,* 432 F.2d 787, 792 (Ct.
(Continued . . .)

Each of the following claim terms – host input register, first input register, system output register, first output register, second output register, system input register and second input register – were added during prosecution of the Chan '241 patent (Ex. 22). Thus, these claim terms must find support in the patent specification as filed, if they are to have any meaning. These claim terms are not defined by, described in, or otherwise supported by the patent specification. Therefore, these terms do not satisfy the written description requirement of 35 U.S.C. § 112 ¶ 1 and are indefinite for failing to satisfy 35 U.S.C. § 112 ¶ 2 (a patentee must "particularly point[ ] out and distinctly claim[ ] the subject matter which the applicant regards as his invention").[46]

P. Indefinite Phrase: "buffering and selective provision of data to and from said cache storage locations by said plurality of registers" ('241 claim 1)

The claim language requires the plurality of registers to perform the function of "buffering and selective provision of data to and from said cache storage locations." The patent specification describes only one register as being capable of performing the buffering and selective provision operation *to* the cache storage locations, the memory write register.[47] The patent specification, however, fails to disclose any register that is capable of performing the function of "buffering and selective provision of data *from* said cache storage locations." This claim phrase is also inconsistent with Chan's use of the term "buffering" in the specification and discussed above at Part IV.H. As discussed above, buffering involves using a register in cache to

(. . . continued)
Cl.1970).

[46] The definiteness of a limitation should be addressed as part of claim construction. *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n,* 161 F.3d 696, 705 (Fed. Cir. 1998).

[47] '709 at 32:39-42 ("[i]n addition, the memory write register 120 can be used as a buffer on write cycles ")

transfer data from one device external to the cache to another external device. In contrast this claim phrase requires "buffering . . . of data . . . from [the internal] cache storage locations." This phrase is flatly at odds with the meaning given to the term by the specification and should be found indefinite. *Amgen*, 314 F.3d at 1342 ("[A]mbiguity in claim scope is at the heart of the definiteness requirement.").

Q. "system memory" - '241 claims 1, 15 and 16

Freescale	ProMOS
main memory of a computer system that is external to the CPU chip	Main memory of a computer, relatively larger and slower than cache memory

Freescale's construction properly recognizes that the main memory like the cache memory and cache controller are external to the host processor. ProMOS's overbroad construction allows for main memory to be internal to a host processor. All descriptions, figures, and embodiments in the specification show that the system memory is external to the processor, and there is no support to the contrary anywhere in the intrinsic evidence. *See, e.g.*, Figure 32. Freescale's proposed construction should be adopted.

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CERTIFICATE OF SERVICE

I hereby certify that on November 6, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

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Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on November 6, 2007 upon the following individuals in the manner indicated:

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TAB 1A

ProMOS Technologies, Inc. v. Freescale Semiconductor, Inc., (D. Del.) CA No. 06-788 (JJF)

11-6-2007

Parties' Proposed Claim Constructions for the Fortin '267 Patent

Fortin Claim Limitation	Freescale's Constructions	ProMOS's Constructions
physical vapor deposition	A process of building up material on a surface in which the material to be deposited is released from a source of the material into a vapor phase by one or more physical mechanisms. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	A process in which films are deposited atomically by means of fluxes of individual neutral or ionic species.
chemical vapor deposition	A process of building up material on a surface in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	A process in which films are precipitated from the gas phase by a chemical reaction.
sputtering	A type of physical vapor deposition in which a solid target is bombarded with high energy ions physically to dislodge the surface atoms on the target into a vapor phase for accumulation on the deposition surface without undergoing a chemical reaction.	A process in which atoms from near the surface of a material are physically dislodged by an incoming ion.
rounding	This term is indefinite.	Reducing the sharpness of the top edge of the opening.

TAB 1B

ProMOS Technologies, Inc. v. Freescale Semiconductor, Inc., (D. Del.) CA No. 06-788 (JJF)

11-6-2007

Parties' Proposed Claim Constructions for the Chan '709 and '241 Patents

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
cache memory apparatus / cache memory	A memory chip that is external to the CPU chip.	Small block of high speed memory associated with a computer processor/ microprocessor (CPU).
host port	A set of pins on the cache memory chip used for the input and output of data over the host data bus.	Interface between a cache memory and a host processor or host data bus.
system port	A set of pins on the cache memory chip used for the input and output of data over the system data bus.	Interface between a cache memory and a system memory or system data bus.
dual port cache memory	A cache memory chip having a host port and a system port.	A cache memory that has two interfaces.
cache controller	A chip that controls a cache chip.	Circuitry that controls the transfer of data or other information to and from cache memory.
controller	A chip that controls a cache chip.	Does not need construction.
first port	Pins on cache controller chip used for the input and output of address information over the host address bus.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a port connected to the host address bus.
second port	Pins on cache controller chip used for the input and output of address information over the system address bus.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a port connected to the system address bus.
host	A single chip central processing unit (CPU)	CPU associated with one or more cache memories.
host microprocessor	A single chip central processing unit (CPU).	CPU associated with one or more cache memories.
host processor	A single chip central processing unit (CPU).	CPU associated with one or more cache memories.
bus	A set of conductors used to transfer data between devices.	Line or set of lines used to transfer data or other information.
host address bus	A set of conductors connected to the address terminal pins of a CPU chip used to transfer memory addresses from the CPU to other components of a computer system.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
host data bus	A set of conductors connected to the data terminal pins of the CPU used to transfer data to and from the CPU and other components of a computer system.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.
buffering	Using a storage element (e.g., memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (e.g., the CPU) to another external device (e.g., system memory) because of differences in rates of data flow or time of occurrence of events.	Storing data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of data.
means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back. register for write back to said system port. Corresponding Structure: the valid bits associated with the memory update register set 116.
means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port. Corresponding Structure: the valid bits associated with the memory update register set 116.
means for masking the providing of selected ones of said words of the fetched data to said random access memory	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: masking the providing of selected ones of said words of the fetched data to said random access memory. Corresponding Structure: the mask bits associated with the memory update register set 116.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
means for masking writing of selected words of data into said random access memory	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: masking writing of selected words of data into said random access memory. Corresponding Structure: the mask bits associated with the memory update register set 116.
means for disabling said dual port cache memory during a local bus access cycle	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: disabling said dual port cache memory during a local bus access cycle. Corresponding Structure: circuitry within the Controller 70 that evaluates host address and control signals and determines when a host bus cycle is not passed on to the system bus and does not cause a cache hit/miss determination. This includes the circuitry within Local Processor Interface Unit 220 and Control Register Interface Unit 224. Operation of the circuitry is described at 42:58-43:42, with reference to Fig. 37 and 38 and in Table VI at 39:27-35.
first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus	Indefinite – no corresponding structure disclosed in the specification.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent that Freescale is suggesting that the term "first control sequencer" needs to be construed, and to the extent the Court decides to construe the term, it means: a first machine which puts items of information into a particular order. (Not means plus function).

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
operations at said system port to be decoupled from said random access memory	Indefinite.	
operably decoupled	Indefinite.	Does not need construction.
register	A set of bits of high-speed memory within an electronic device, used to hold data for a particular purpose.	Circuitry capable of retaining data or other information, such as address information
host input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: (in claim 10) a register connected to the host port (in claim 15) a register coupled to the addressable memory storage and the host data bus.
system input register	Indefinite.	
system output register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register connected to the system port.
first input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for selectively writing input data to the addressable storage.
first output register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for selectively furnishing output data to the system port.
second input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for providing second input data to the addressable storage.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
a data path between said host data bus and said system data bus is operably decoupled by buffering and selective provision of data to and from said cache storage locations by said plurality of registers so as to allow concurrent transfer of data to and from said dual port cache memory	The claim phrase "operably decoupled by buffering and selective provision of data to and from said cache storage locations by said plurality of registers" is indefinite.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. See ProMOS's position on "operably decoupled", "buffering," "selective provision", "plurality of registers" and "to allow", above. The term "data path" is clear on its face and does not require construction.
system memory	Main memory of a computer system that is external to the CPU chip	Main memory of a computer, relatively larger and slower than cache memory.
first input data being provided to said random access memory from said memory write register at the same time that the first output data is provided by said write back register to said system port	Whenever the first input data is provided to the RAM, the first output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.
wherein the input data is provided to said random access memory from said memory write register at the same time that the output data is provided by said write back register to said system port	Whenever input data is provided to the RAM, output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "is provided" and "at the same time" need to be construed, these terms are clear on their face.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
said input data being provided to said addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port	Whenever the input data is provided to the addressable storage, the output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.
said second input data being provided to said addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port	Whenever the second input data is provided to the RAM, the second output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.
selectively providing input data received from said host port to one of said random access memory, said system port, and said random access memory and said system port	Providing input data received from the host port to: said random access memory and not to said system port under one set of conditions, said system port and not to said random access memory under a second set of conditions, and said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "host port" and "system port" and ProMOS's position on "selectively providing" and "random access memory."
selectively providing	Providing data held in a register depending on certain conditions and never providing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: providing on a selective basis.
selective provision	Providing data held in a register depending on certain conditions and never providing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: provision on a selective basis.
selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port	Providing the first data to: said random access memory and not to said system port under one set of conditions, said system port and not to said random access memory under a second set of conditions, and said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above, and ProMOS's position on "selectively providing" and "random access memory above.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
selectively furnishing first output data to said system port	Furnishing first output data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing first output data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.
selectively providing second input data to said random access memory	Providing second input data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never providing second input data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively writing" below and its position on "random access memory."
selectively furnishing write back data to said system port	Furnishing data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing data received from the RAM depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.
selectively providing memory write data to one of said random access memory, said system port via said bypass path, and said random access memory and said system port via said bypass path	Providing data buffered in the memory write register from the host port to: -said random access memory and not to said system port under one set of conditions, -said system port via said bypass path and not to said random access memory under a second set of conditions, and -said random access memory and said system port via said bypass path under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" and its position on "selectively providing" and "random access memory."
selectively providing system fetch data to said random access memory	Providing system fetch data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never providing system fetch data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively providing" and "random access memory."
selectively writing	Writing data held in a register depending on certain conditions and never writing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: writing on a selective basis.
selectively furnishing	Furnishing data held in a register depending on certain conditions and never furnishing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe anyway, it means: furnishing on a selective basis.

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TAB 2A
SELECTIVELY PROVIDING PHRASES

FREESCALE'S PROPOSED CONSTRUCTION	PROMOS'S PROPOSED CONSTRUCTION
Selectively providing (Chan '709: 1, 13, 17, 22)	
providing data held in a register depending on certain conditions and never providing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe the term anyway, it means: providing on a selective basis.
Selective provision (Chan '241:1)	
providing data held in a register depending on certain conditions and never providing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe the term anyway, it **means: provision on a selective basis.**
selectively providing second input data to said random access memory (Chan '709: 17)	
providing second input data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never proving the data held depending on other conditions	**Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively providing" and "random access memory."**
selectively providing system fetch data to said random access memory (Chan '709: 22)	
providing data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never providing the data held depending on other conditions	**Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively providing" and "random access memory."**
Selectively writing first input data to said random access memory (Chan '709: 17)	
writing data received from the host port and held in the memory write register to said random access memory depending on certain conditions and never writing the data held depending on other conditions	**Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively writing" below and its position on "random access memory."**
selectively furnishing first output data to said system port (Chan '709: 17)	
furnishing data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing the data held depending on other conditions	**Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.**
selectively furnishing write back data to said system port (Chan '709: 22)	
furnishing data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing the data held depending on other conditions	**Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.**

selectively furnishing (Chan '241: 16)	
furnishing data held in a register depending on certain conditions and never furnishing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe anyway, it **means: furnishing on a selective basis.**
selectively writing (Chan '241: 16)	
Writing data held in a register depending on certain conditions and never writing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe the term anyway, it **means: writing on a selective basis.**

TAB 2B

SELECTIVELY PROVIDING TO ONE OF [A], [B] AND [C] PHRASES

FREESCALE'S PROPOSED CONSTRUCTION	PROMOS'S PROPOSED CONSTRUCTION
Selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port (Chan '709: 1)	
providing the first data to: -said random access memory and not to said system port under one set of conditions, -said system port and not to said random access memory under a second set of conditions, and -said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above, and ProMOS's position on "selectively providing" and "random access memory above.
selectively providing input data received from said host port to one of said random access memory, said system port, and said random access memory and said system port (Chan '709: 13)	
providing input data received from the host port to: -said random access memory and not to said system port under one set of conditions, -said system port and not to said random access memory under a second set of conditions, and -said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "host port" and "system port" and ProMOS's position on "selectively providing" and "random access memory."
selectively providing memory write data to one of said random access memory, said system port via said bypass path, and said random access memory and said system port via said bypass path (Chan '709: 22)	
providing data buffered in the memory write register from the host port to: -said random access memory and not to said system port under one set of conditions, -said system port via said bypass path and not to said random access memory under a second set of conditions, and -said random access memory and said system port via said bypass path under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" and its position on "selectively providing" and "random access memory."

TAB 2C

AT THE SAME TIME CLAIM PHRASES

FREESCALE'S PROPOSED CONSTRUCTION	PROMOS'S PROPOSED CONSTRUCTION
the input data is provided to said random access memory from said memory write register at the same time that the output data is provided by said write back register to said system port (Chan '709: 13)	
Whenever the the input data is provided to the RAM, the output data must be provided to the system port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.**
first input data being provided to said random access memory from said memory write register at the same time that the first output data is provided by said write back register to said system port (Chan '709: 17)	
Whenever the first input data is provided to the RAM, the first output data must be provided to the system port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.**
the second input data being provided to said random access memory from said memory update register at the same time that the second output data is provided by said read hold register to said host port (Chan '709: 17)	
Whenever the second input data is provided to the RAM, the second output data must be provided to the host port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.**
said input data being provided to said addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port (Chan '241: 16)	
Whenever the input data is provided to the addressable storage, the output data must be provided to the system port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.**

said second input data being provided to said addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port (Chan '241: 16)	
Whenever the second input data is provided to the RAM, the second output data must be provided to the system port	**Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.**

TAB 2D

MEANS-PLUS-FUNCTION CLAIM PHRASES

FREESCALE'S PROPOSED CONSTRUCTION	PROMOS'S PROPOSED CONSTRUCTION
means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port (Chan '709: 10) means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port (Chan '709: 26)	
Indefinite – no corresponding structure disclosed in the specification	Means plus function. Function: identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port Corresponding Structure: the valid bits within the memory update register set 116
means for masking the providing of selected ones of said words of the fetched data to said random access memory (Chan '709: 12) means for masking writing of selected words of the system fetch data into said random access memory (Chan '709: 21, 24) means for masking writing of selected words of data into said random access memory (Chan '241: 26)	
Indefinite – no corresponding structure disclosed in the specification	Means plus function. Function: masking the providing of selected ones of said words of the fetched data to said random access memory Corresponding Structure: the mask bits within the memory update register set 116
means for disabling said dual port cache memory during a local bus access cycle (Chan '241: 5, 19)	
Indefinite – no corresponding structure disclosed in the specification **- no antecedent for local bus**	Means plus function. Function: disabling said dual port cache memory during a local bus access cycle Corresponding Structure: the logic inside Controller 70 that determines when to assert KEN

first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus (Chan '241: 4, 18)	
Indefinite – no corresponding structure disclosed in the specification	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent that Freescale is suggesting that the term "first control sequencer" needs to be construed, and **to the extent the Court decides to construe the term, it means: a first machine which puts items of information into a particular order. (Not means plus function).**
a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus (Chan '241: 4, 18)	
Indefinite – no corresponding structure disclosed in the specification	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent that Freescale is suggesting that the term "second control sequencer" needs to be construed, and to the extent the Court decides to construe the term, it means: a second machine which puts items of information into a particular order. **(Not means plus function).**

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